CoolSiC™

How Infineon controls and assures the reliability of SiC based power semiconductors

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1 Introduction

Infineon's CoolSiC™ trench based silicon carbide power MOSFETs represent a dramatic improvement in power conversion switching device Figure Of Merit (FOM) values with outstanding system performance. This enables higher efficiency, power density and reduced system cost in many applications. This technology can also be considered as being an enabler for new applications and topologies.

However, as with all new technologies, it is essential that a thorough technology development and product qualification procedure is followed. Only in this way can design lifetime and quality requirements for power conversion systems be achieved. Despite the similarities to silicon, e.g. the vertical device structures, the presence of a native oxide like SiO_2 or the majority of processing steps, there are still important differences related to the material properties itself and the operating modes of these new power devices. As these differences are substantial, their impact on the operation in the final application and on the required development and reliability qualification processes must be carefully considered.

This paper describes the major steps in the release process that Infineon has used to successfully qualify CoolSiC™ technology and products. Key failure mechanisms are described, and the means to ensure safe and reliable operation in a wide variety of applications are provided.

Through this approach, many risks our customers would otherwise encounter are avoided and a safe path to the reliable use of Infineon CoolSiC™ technology is provided. This publication also holds tutorial value to engineers with an interest in better understanding silicon carbide related reliability.

2 Why do SiC based devices require some additional and different reliability tests compared to Si based devices?

One of the success factors of implementing SiC as a power device material is the chance to adopt many of the well known device concepts and processing technologies from silicon. Among those are the basic device designs like vertical Schottky diodes or vertical power MOSFETs (after some detours via JFETs and BJT's as alternative structures). Thus, many of the procedures used to verify the long term stability of silicon devices could be transferred to SiC. Nevertheless a deeper analysis has shown that SiC based devices require some additional and different reliability tests compared to Si based devices. The major items which turned out to be relevant are the following:

- The material itself with its specific defect structures, anisotropies, mechanical and thermal properties etc.
- The larger bandgap with its implications on the density and dynamics of interface traps in MOS based devices
- Up to about 10x higher electrical fields in operation within the material itself and at the outside interfaces, e.g. device edges (including new edge termination designs), plus its impact on oxide lifetime
- New operating modes where high voltage operation (V_{DS} > 1000 V) and fast switching (> 50 V/ns) are combined

The listed items may have an influence on nearly all established qualification tests. Power cycling second tests will lead to different results due to different mechanical properties. Contrary to silicon based power devices the setup of oxide reliability tests for SiC have to also cover stability in blocking mode. Furthermore, for many existing qualification standards that specify accelerated tests, models are used to extrapolate the test data and correlate it to real world application conditions. These model parameters need to be verified for their application and accuracy with respect to SiC.

Infineon has intensely analyzed all of these items over the last 25 years during the development and production of SiC based power devices. New tests have been developed to address different operating modes not seen by silicon power semiconductors and other tests have been modified to take into account SiC specific requirements. It is important to emphasize, that key parts of the characterization and validation scheme are based on a mission profile based stress analysis. This was done in order to assess the critical operating conditions for SiC devices and to understand new potential failure mechanisms.

The details are described in the following chapters.

3 Gate-oxide reliability of industrial SiC MOSFETs – FIT rates and lifetime

3.1 Introduction to gate oxide reliability for SiC MOSFETs

High numbers of early gate-oxide failures have hampered the commercialization of SiC MOSFETs for many years, and provoked skepticism whether SiC MOS switches would ever be as reliable as their Si counterparts. During the last decade, SiC technology has substantially matured and SiC MOS devices have exhibited gradual improvements in gate-oxide reliability. This has opened the door for their successful introduction into the mass market.

In the field of gate-oxide reliability, there is a lot of expertise that can be reused from Si technology. For instance, it was shown that the physical breakdown strength of SiO_2 on SiC is similar, if not identical, to SiO_2 on Si [1]. This means that the overall breakdown stability of SiO_2 fabricated on SiC is as good as SiO_2 fabricated on Si. The shortcoming in gate-oxide reliability of SiC MOSFETs with respect to Si MOSFETs is due to “extrinsic” defects. Extrinsic defects are tiny distortions in the gate-oxide, which act as local oxide thinning, cf. Figure 1.

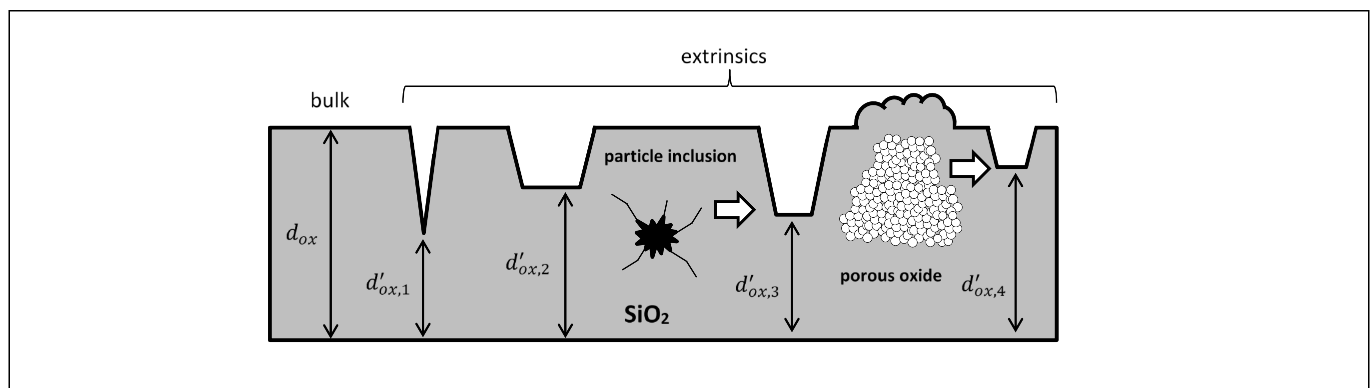

Figure 1 Schematic representation of extrinsic defects in SiO_2. Extrinsic defects can be physical oxide thinning due to, for instance, a distorted oxide on top of an EPI/substrate defect or electrical oxide thinning caused by a degraded dielectric field strength due to inclusions of metallic impurities, particles or porosity [2].

Such distortions may originate from EPI or substrate defects [2], metallic impurities, particles or other extrinsic inclusions in the gate-oxide incorporated during device fabrication.

3.2 Basic aspects of SiC MOSFET gate-oxide reliability screening

At the end of processing, gate-oxides fabricated on SiC have typically a much higher early failure probability because they exhibit higher numbers of extrinsic defects, cf. Figure 2.

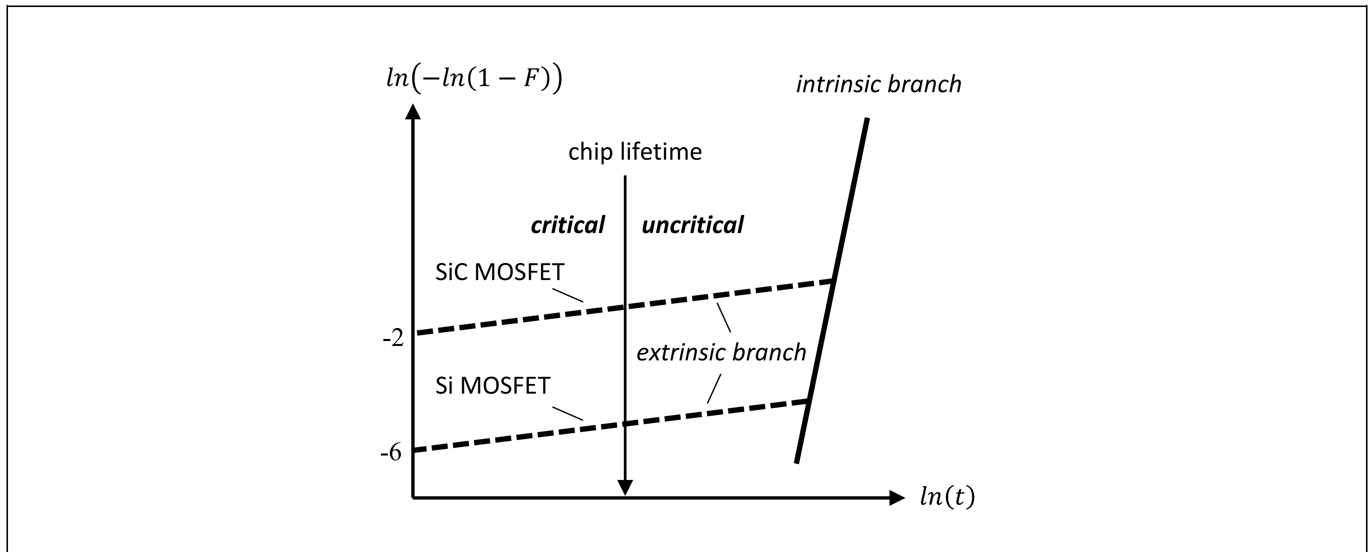

Figure 2 Schematic representation of the extrinsic and intrinsic Weibull distributions for SiC MOSFETs and Si MOSFETs having the same oxide thickness and area. F depicts the cumulative failure probability, t the time. Due to a higher electrical defect density, SiC MOSFETs exhibit 3-4 orders of magnitude higher extrinsic defect densities in the gate-oxide. The chip lifetime is the time the device has to survive in the application under normal use conditions.

To make SiC MOSFETs as reliable as their Si counterparts, the gate-oxide defect density has to be minimized during processing. Additionally, innovative screening techniques, to identify and eliminate potentially weak devices, e.g. in the electrical end test, have to be developed. The screening of weak devices in the end test is typically done by subjecting each device to a high gate-voltage stress pulse with defined amplitude and time [3] [4]. The stress pulse is designed to identify devices with critical extrinsic defects while devices without extrinsic defects or with only non-critical extrinsic defects survive. The remaining surviving, screened, population shows a significantly improved gate-oxide reliability [5].

The enabler for a fast and efficient gate-voltage screening is a much thicker bulk-oxide layer than what is typically needed to fulfill intrinsic lifetime-targets. The thicker bulk-oxide layer allows the use of screening voltages much higher than the typical device use-voltage without degradation of non-defective devices which are passing the screening test. The higher the screening voltage to the use-voltage ratio, the more efficient the electrical screening [6]. By eliminating defective devices in the end test a potential reliability issue for the customer is converted to a minor yield loss for the device manufacturer. SiC MOSFETs that pass our screening test show the same excellent level of gate-oxide reliability as Si MOSFETs or IGBTs [7].

The downside of a thicker bulk-oxide layer is a slightly higher MOS channel resistance. The MOS channel resistance is directly proportional to the gate-oxide thickness and can be a major portion of the total on-resistance, in particular, for devices of lower voltage classes that provide a comparatively small drift-zone resistance. Ultimately, high screening efficiency, and hence excellent gate-oxide reliability of SiC MOSFETs, is not entirely for free, but comes at the cost of a slightly increased on-resistance. This design trade-off between reliability and performance is inevitable, however, it is possible to take advantage of the fact that on-resistance and gate oxide reliability show a different dependence on bulk oxide thickness.

While gate oxide reliability improves exponentially with oxide thickness, the on-resistance increase is only linear. At elevated temperatures, where the drift-zone resistance is more pronounced, the performance penalty is even smaller in relative numbers. To summarize, by sacrificing just a little performance by using a thicker bulk-oxide layer leads to a strong gain in reliability. Infineon decided, from the beginning, to use a Trench based MOSFET technology. The reason for this is that trench based devices, compared to planar devices, have significantly higher channel conductivities at low electric fields across the gate oxide during on-state of a MOSFET as the penalty of a thick oxide layer.

A not very attractive alternative to gate voltage screening at high screening voltages and room temperature is the classic burn-in test. During burn-in devices are typically stressed at somewhat lower gate voltages and elevated temperatures for much longer times. This approach has several disadvantages. A burn-in is time-consuming, costly, and may cause severe drift of threshold voltage and on-resistance due to long-lasting gate stress at high bias and high temperature, which is known to trigger bias temperature instabilities [8].

3.3 Stress tests for extrinsic gate-oxide reliability evaluation

To make reliable predictions about failure probabilities under normal device operation conditions, it is mandatory to perform stress tests that explore the early breakdown regime of device failure [9]. Stress tests aiming to explore the oxide wear-out regime, such as highly accelerated Time-Dependent-Dielectric-Breakdown (TDDB) tests which are typically performed only on a small number of samples, are not appropriate to study failures that may happen during normal device operation (voltage, temperature) within typical chip lifetimes. To overcome this problem, Infineon developed two different stress test approaches to verify the screening and thereby the gate oxide reliability for all devices.

3.3.1 Marathon stress test

A common approach to study extrinsic failures is to stress devices as close as possible to the real world application conditions and at the same time test large numbers of samples. Large sample sizes are required because extrinsic failures are usually rare, in particular, after electrical screening. For this purpose, we have developed a new kind of test procedure, which we call the “marathon stress test” [5]. In this test, thousands of devices are stressed in parallel in a parameter range close to operating conditions and comparable to typical burn-in conditions. However, contrary to burn-in, we use much longer stress times (100 days) in order to increase the probability to find extrinsic failures. To manage the large sample quantities required for the marathon stress test, we have developed a special test setup in which we put multiple devices in one package, many packages on one stress board and several stress boards into one furnace. Multiple furnaces are can be operated in parallel.

In a case study, we have performed three independent marathon test runs on three sample groups of electrically screened devices with different extrinsic defect densities. The three groups roughly align with the progress made during the device development phase, namely group 1 corresponds to the initial stage of oxide process development while group 3 represents the technology status shortly before

product release. The purpose of the experiment was to monitor and quantify the efficiency of various improvements in cleaning, processing and electrical screening. Within 100 days at 150°C, the best group (group 3) showed only one failure out of 1000 devices at V_{GS} = +30 V and 0 failures at V_{GS} = +25 V and V_{GS} = -15 V. The failures in the marathon stress tests are illustrated as Weibull distributions in Figure 3. To get the corresponding Weibull distributions at operating conditions, we converted the times to failure at V_{GS} = +30 V to times to failure at V_{GS} = +18 V using the linear E-model [9] [10]. The result of the conversion is depicted in the upper right corner of Figure 3. Note that all failures observed in the 30 V marathon test run would have happened far beyond an assumed specified product lifetime of 20 years at a nominal gate bias of 18 V. The failure probability during one lifetime can be deduced by extrapolating the measurement data to an assumed maximum operation time of, for instance, 20 years.

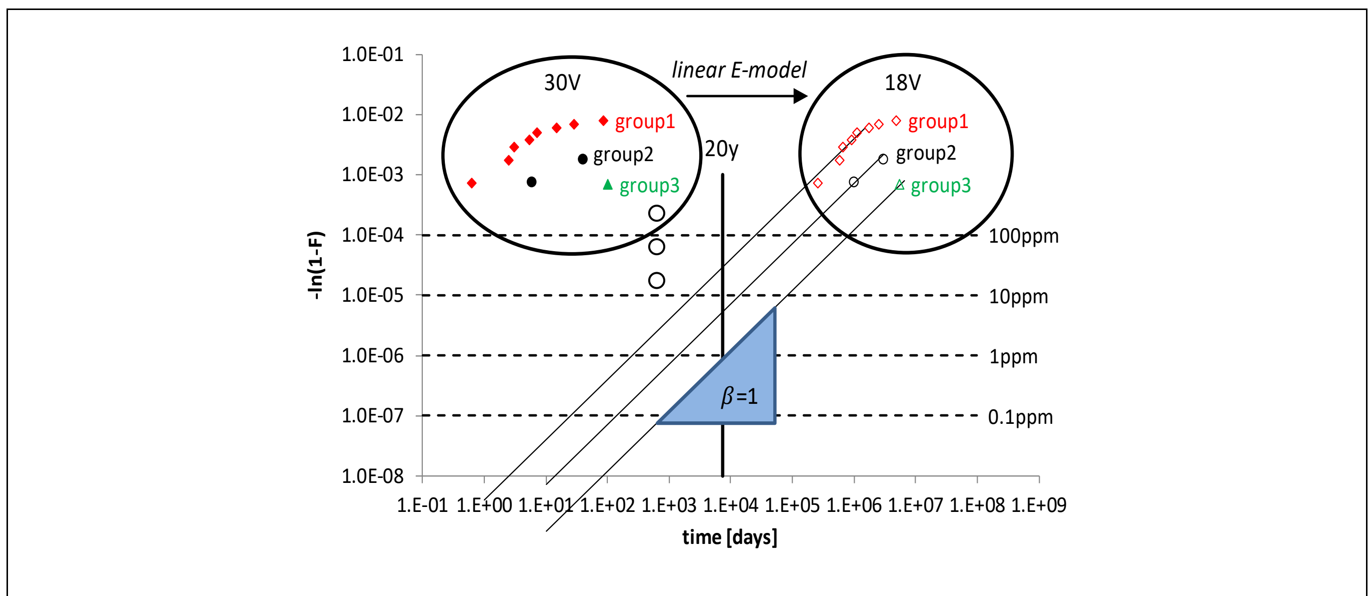

Figure 3 Weibull plots of failure probabilities in the marathon test for the three different SiC trench MOSFET sample groups with different extrinsic defect densities. The marathon test results obtained at V_{GS} = 30 V overstress were converted to a gate use-voltage of V_{GS} = 18 V using the linear E-model. For F and t please refer to the explanation in Figure 2.

For the extrapolation we assumed a Weibull slope parameter of β = 1. This is a state-of-the-art approach for failure rate analysis where, after screening is performed to eliminate the extrinsic failures, the resulting population failure probability follows a Weibull slope of 1 for intrinsic failures. [5] [6]. Summarizing the final result of the marathon test case study: two out of the three groups show single digit ppm failure probabilities for 20 years operation at 18 V and 150°C. These values are comparable to established Si technologies.

The marathon stress test is a very powerful methodology to estimate lifetime failure probabilities of SiC MOSFET device populations during normal device operation. However, the test requires large sample sizes and needs to be calibrated in a very sophisticated manner. Gate stress levels have to be chosen far below the intrinsic breakdown limit of the tested devices but still harsh enough to trigger a few extrinsic failures within the planned duration of the test. The definition of suitable stress conditions

requires extensive preliminary investigations and/or a considerable knowledge of the devices under test. Because of that and due to the special test setup needed for paralleling, the marathon stress test is mainly useful for device manufacturers to quantify the reliability of SiC MOSFETs produced in their own fab. For a more qualitative comparison of gate-oxide reliability of different manufacturers an end-of-life stress test such as the “gate voltage step-stress test” is more convenient [6] [10] [11].

3.3.2 Gate voltage step-stress test

In this test a smaller number of SiC MOSFET devices, e.g. 100 parts, are tested at the maximum allowed junction temperature ($T_{j,max}$) for a defined stress time (t_{str}), e.g. 24 h or 168 h, using a stepped increase in gate stress bias, c.f. Figure 4. After each step increase in stress level, devices are checked for gate-source leakage current levels. Failing devices are counted and removed from the distribution. In a first stress step devices are biased at the recommended gate use voltage ($V_{GS,rec}$), e.g. +15 V. The second stress step is performed in the same way as the first one but at the maximum allowed gate voltage ($V_{GS,max}$). From this step on the test is continued by increasing the gate voltage by e.g. +2 V after each stress step until all devices have failed ($V_{GS,EOL}$). At the end of the test, time and number of failed devices are analyzed using Weibull statistics. An example is given in Figure 5 which displays a comparison of tests performed on devices from four different SiC MOSFET suppliers. The plot shows that only M4 shows a clean intrinsic branch with an adequate failure rate assuming an operating time of 20 years while other components, mainly M1, show significantly higher numbers of extrinsic failures at relatively low electric fields.

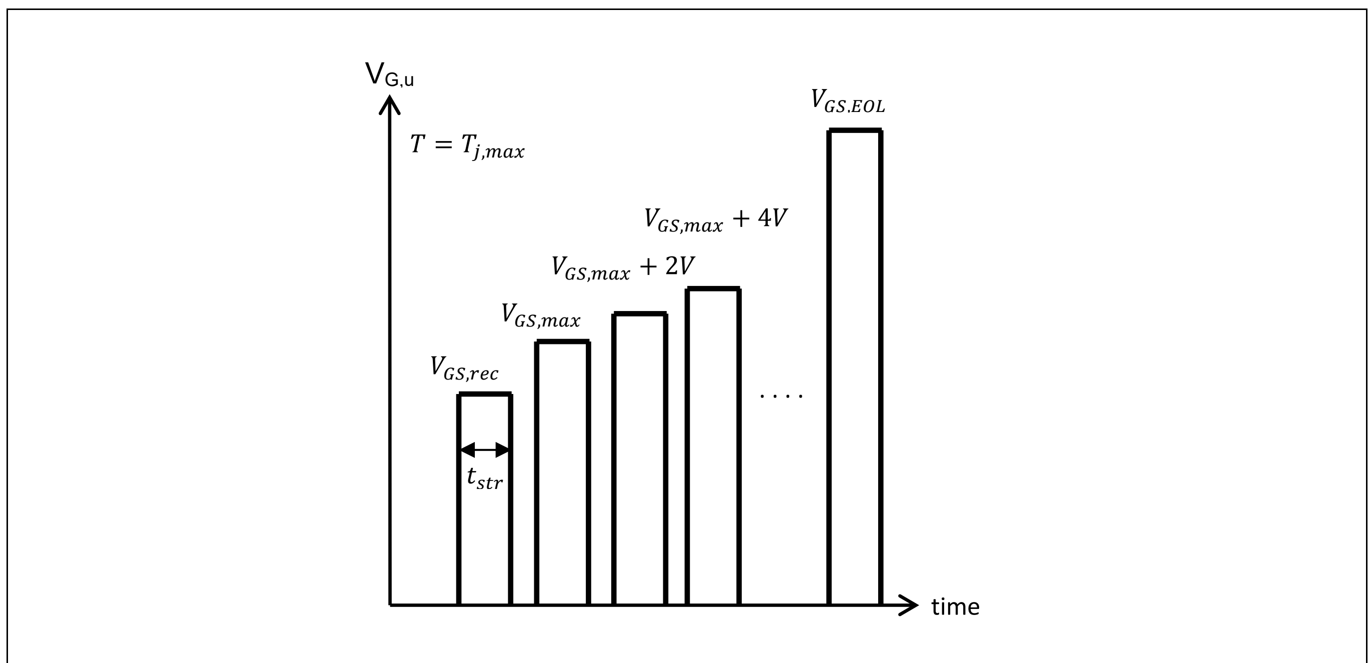

Figure 4 Gate voltage step-stress test. Before and after each stress sequence, the gate integrity of each chip is checked via a gate-source leakage test. The procedure is an end-of-life test.

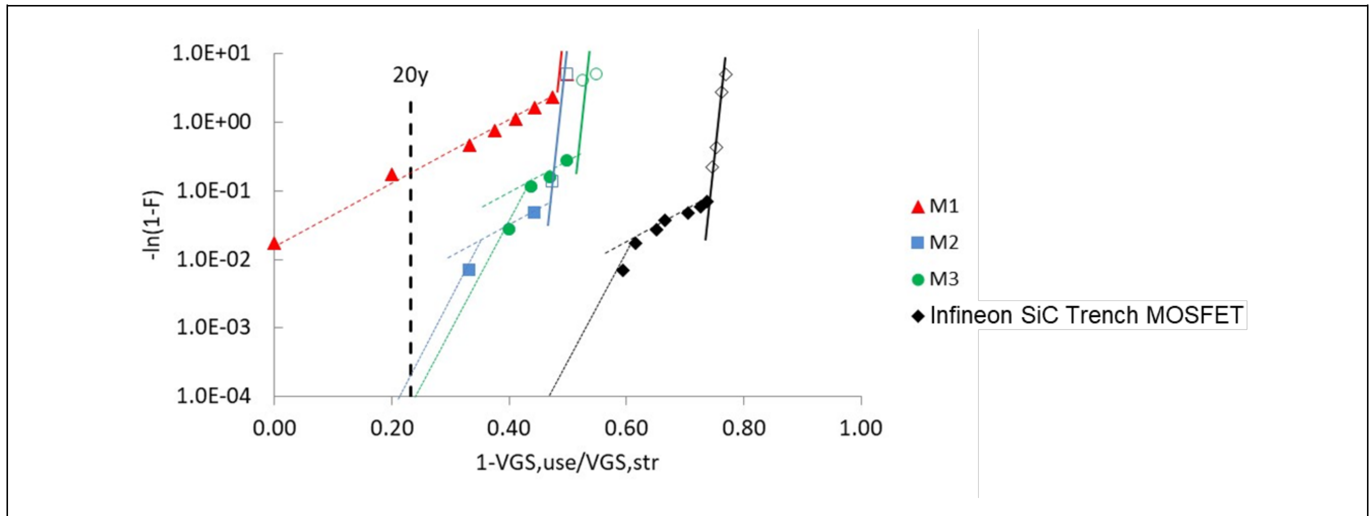

Figure 5 Weibull plot of failures in gate voltage step-stress test from 100 commercially available SiC MOSFET devices of 4 different device manufactures including Infineon's Trench based device using a thicker gate oxide compared to the planar based M1.M3 parts. The open symbols correspond to devices which break down intrinsically, the full symbols correspond to devices with break down extrinsically. The dashed lines indicate the extrinsic branches, the straight lines the intrinsic branches.

3.4 Conclusions

Gate-oxide reliability of SiC MOSFETs has substantially improved. However, due to larger defect densities of the SiC material, it is still challenging to advance toward the "Si standard", i.e. a single digit ppm-rate. This chapter has introduced basic aspects of SiC MOSFET gate-oxide reliability and has outlined the concept of field-failure probability reduction by means of electrical gate voltage screening. To estimate the maximum field-failure probability of industrial SiC trench MOSFETs under typical operation conditions, we have suggested a marathon stress test that is based on a large number of devices that are stressed at voltages close to the operating voltage. The results of the test indicate that excellent gate-oxide reliability (comparable to Si devices) can be achieved with industrial SiC MOSFETs using optimized device processing and efficient electrical screening.

To compare gate-oxide reliability of a limited number of devices with largely unknown gate-oxide properties, e.g. commercial devices of different manufacturers, we have introduced a second more generic end-of-life stress test. This second test does not provide the same predictive power as the marathon stress test but is particularly useful to obtain reliability comparisons of arbitrary SiC MOSFETs from different manufacturers.

4 Gate-oxide reliability of industrial SiC MOSFETs – Bias Temperature Instabilities (BTI)

During normal device operation the threshold voltage of SiC MOSFETs may drift slightly due to generation and/or charging of point defects at or near to the semiconductor-oxide interface. A drift of the threshold voltage can have depending on its amount a strong impact on the long term operation of the device. Since the drift usually is an increase towards higher values it results in an increase of the on resistance of the part as long as the applied V_{GS_ON} remains constant. Thus, losses increase and the device becomes hotter which might degrade the lifetime. Consequently, it is of utmost importance to understand the behavior of the threshold voltage and to consider the effects in datasheet margins and/or design margins.

The phenomenon is well-known from Si technology and called Bias Temperature Instability (BTI). Because of the fact that SiC is a wide bandgap semiconductor, which consists not only of Silicon (Si) but also of Carbon (C) atoms, the SiC/SiO_2 interface has somewhat different properties as compared to the Si/SiO_2 interface. At the SiC/SiO_2 interface other point defect types exist within a larger energy range that need to be passivated by alternative post oxidation schemes (e.g. nitric-oxide instead of forming gas anneals). Furthermore, the wider bandgap of SiC facilitates charge carrier exchange between the semiconductor and the SiO_2 gate-oxide. Naturally, these differences involve slightly modified electrical characteristics and drift dynamics when compared to Si MOSFETs.

A lot of effort has been put into improving the performance of SiC MOSFETs, however, performance improvements do not necessarily correlate with better device reliability [12]. To guarantee stable device characteristics over time, careful attention has to be paid to drift phenomena such as BTI. At Infineon, we strive for best-in-class device performance while at the same time providing excellent device reliability. Thus, intensive studies have been performed in order to develop a deep understanding of the underlying effects, to assess the impact of BTI effects in real applications and to develop measures to suppress BTI as much as possible.

4.1 Parameter variations of SiC MOSFETs under constant gate bias conditions (DC BTI)

4.1.1 Introduction to DC BTI

DC BTI is an effect which is not only observed in SiC power devices but also well-known in silicon (Si) technology. When applying a constant DC bias to the gate of a Si or SiC MOSFET at elevated temperatures, a shift in threshold voltage and on-resistance may be observed. The amplitude and polarity of the shift depends on the stress condition (bias, time, temperature). For positive gate bias stress (PBTI), commonly a shift towards higher threshold voltages is observed whereas for negative gate bias (NBTI) a shift in the opposite direction occurs. The effect is due to charge carrier trapping at or close to the interface between SiC/SiO_2 or Si/SiO_2 and may be minimized by optimized device processing. In order to better understand and predict DC BTI in SiC MOSFETs, Infineon has researched this topic in

depth with an emphasis on the differences with respect to Si technology. In Si MOSFETs Infineon has acquired in the past a solid understanding of BTI and has substantially contributed to scientific progress in collaboration with renowned university partners [13] [14] [15]. The acquired know-how on the degradation physics and electrical measurement techniques has now been transferred to Infineon SiC devices [16] [17]. Indeed, many similarities regarding DC BTI exist in Si and SiC technologies despite the different material properties [18]. However, a few aspects are different and have to be considered in order to correctly measure and assess application relevant parameter variations.

4.1.2 Measuring DC BTI in SiC power devices

Threshold voltage variations caused by DC BTI consist of two components: one fast, recoverable component and one quasi-permanent (very slow recovery) component [19] [20]. The quasi-permanent component determines the long-term drift of a device whereas the fast component recovers in the short term.

In order to obtain comparable drift values, industrial standards on the determination of BTI drift have been developed, such as e.g. JESD22 [21] and its extension AEC-Q101 [22]. These standards were based on Si technology and need to be refined for SiC technology as will be outlined below.

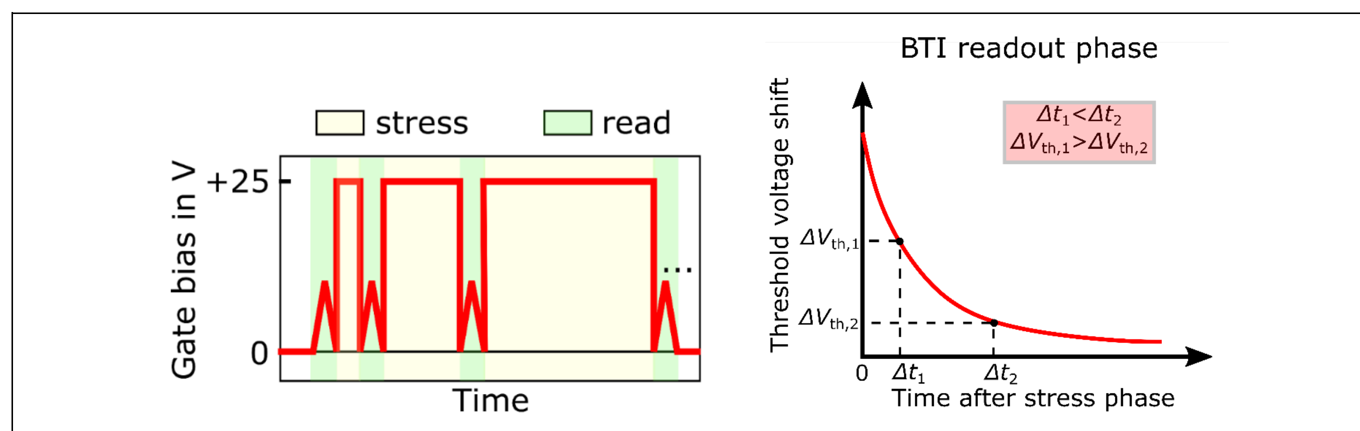

Figure 6 Typical DC BTI MSM (Measure-Stress-Measure) sequence using the example of a PBTI (Pulsed BTI) stress. On the left side, the measurement signal over time is displayed. The right hand side shows the time dependent recovery of the threshold voltage drift, illustrating the influence of readout delays on the extracted threshold voltage shift. Even small differences in readout timing may lead to large variations of the extracted threshold voltage drift.

The traditional way of measuring DC BTI is a Measure-Stress-Measure (MSM) sequence consists of a repeated applied gate bias and temperature stress followed by a readout Figure 6, left hand side. With this method and appropriate equipment, it is possible to measure both drift components mentioned above. However, the obtained threshold voltage shift strongly depends on the readout timing, i.e. the delay between the stress and the readout phase, and the device history [19] [23]. As can be seen in Figure 6 right, the threshold voltage drift recovers exponentially after termination of stress. Thus, even small differences in the readout timing, e.g. 1 ms vs. 100 ms, may lead to large variations in the

extracted threshold voltage drift. As a consequence, this simple technique involves poor reproducibility and difficulties in distinguishing between fully recoverable fast components (hysteresis effects) and more application relevant quasi-permanent components of threshold voltage shift.

For this reason, Infineon suggests to use a modified BTI measurement sequence with preconditioning pulses, as is shown in Figure 7. Using the example of preconditioned PBTI, the readout phase consists of an accumulation pulse, a first readout at a fixed current level, an inversion pulse and a second readout. After the full sequence, i.e. in the second readout, mainly the quasi-permanent BTI component is left, which shows almost no or very slow recovery. This means that the preconditioning makes the measurement more reproducible, less sensitive to readout delays and device history and allows to correctly differentiate between hysteresis and drift effects [19].

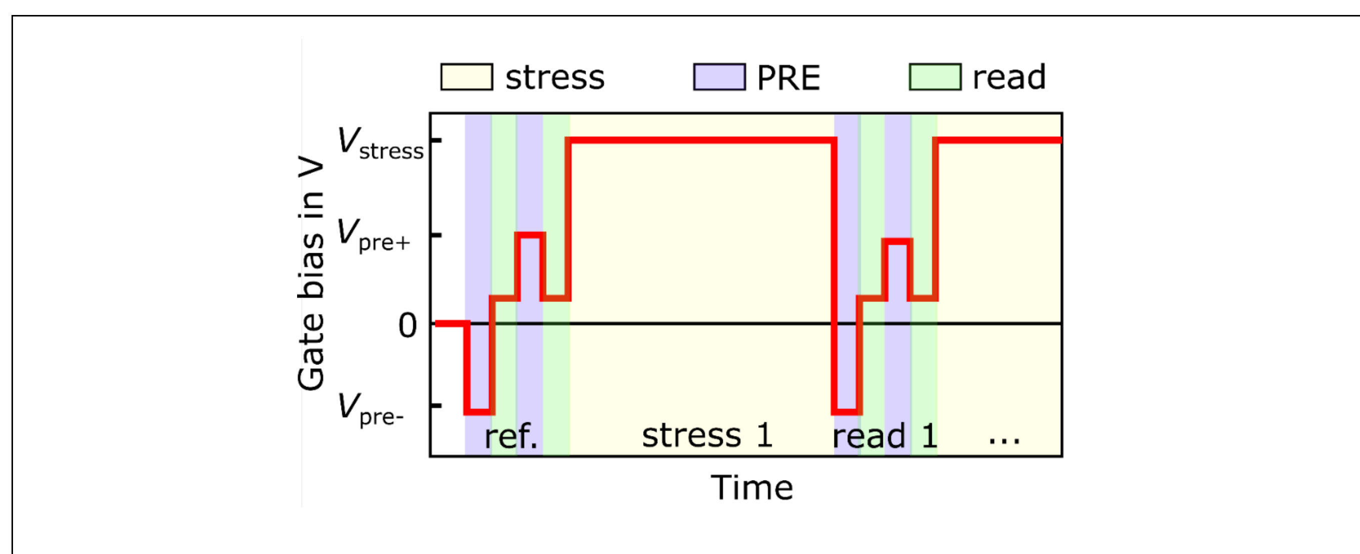

Figure 7 Measurement sequence for preconditioned PBTI. The readout phase consists of an accumulation pulse, a first readout, an accumulation pulse and a second readout. The second readout yields in the most stable and reproducible results over time.
The difference between the first and second readout within a single readout phase represents the threshold voltage hysteresis. Its drift over time is a measure for the generation of new interface states. The preconditioning pulses mimic the switching of the gate in the application and bring the trap states into a defined charge-state, thereby reducing the influence of readout delays and device history.

4.1.3 Comparison of DC BTI in SiC and Si power MOSFETs

In older publications, often significantly higher drifts were reported for SiC MOSFETs than for Si power devices (e.g. [24]). In contrast, we have demonstrated the low NBTI drift levels (negative BTI) of our SiC power MOSFETs which are comparable to state-of-the art Si superjunction MOSFETs (even for a significant overstress of the devices). This result has been achieved by optimizing device processing. For SiC, several different process variants are presented in order to demonstrate the potential of improving or degrading BTI by means of SiC/SiO_2 interface engineering.

4.1.3.1 Negative Bias Temperature Instability (NBTI)

Infineon studied the NBTI drift at 200°C for a stress bias of -25 V (Figure 8). It was possible to reduce the NBTI drift of our SiC MOSFETs by one order of magnitude by several process improvements. Within the experimental window of the test the resulting NBTI drift levels of the best process variants are in the same order of magnitude as the Si MOSFET. The drift slope of the SiC MOSFETs is even smaller indicating less drift than the Si MOSFET at longer stress times. The low NBTI is a characteristic feature of Infineon's SiC MOSFETs.

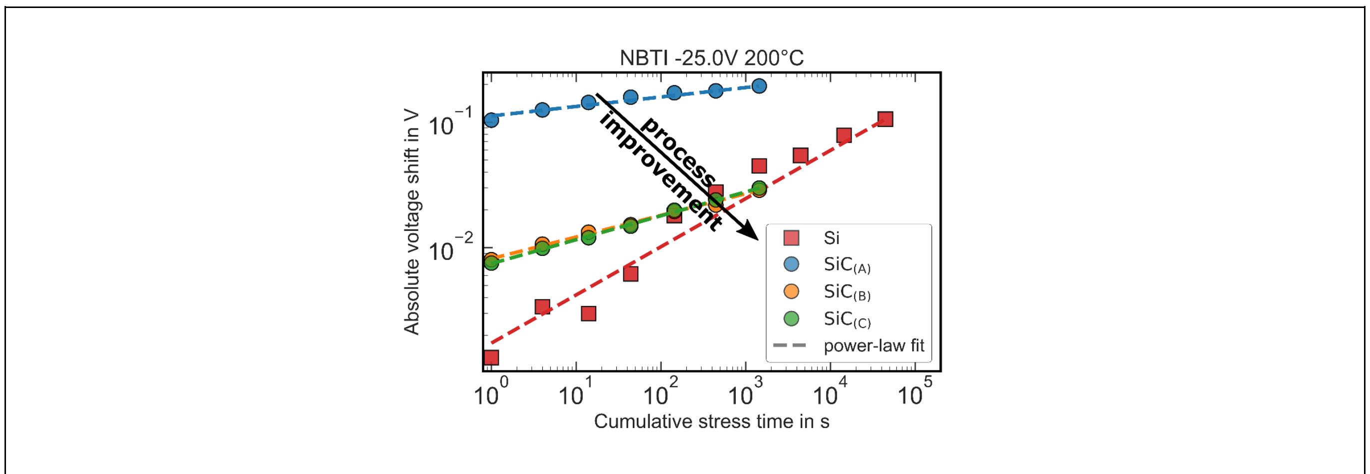

Figure 8 NBTI time evolution at 200°C using a stress bias of -25 V. By process improvements, the total drift of our SiC MOSFETs could be reduced to a similar level as for comparable Si power MOSFETs.

4.1.3.2 Positive Bias Temperature Instability (PBTI)

We studied the PBTI drift at 200°C for a stress bias of +25 V (Figure 9). PBTI in Si and SiC show many similarities and only a few differences.

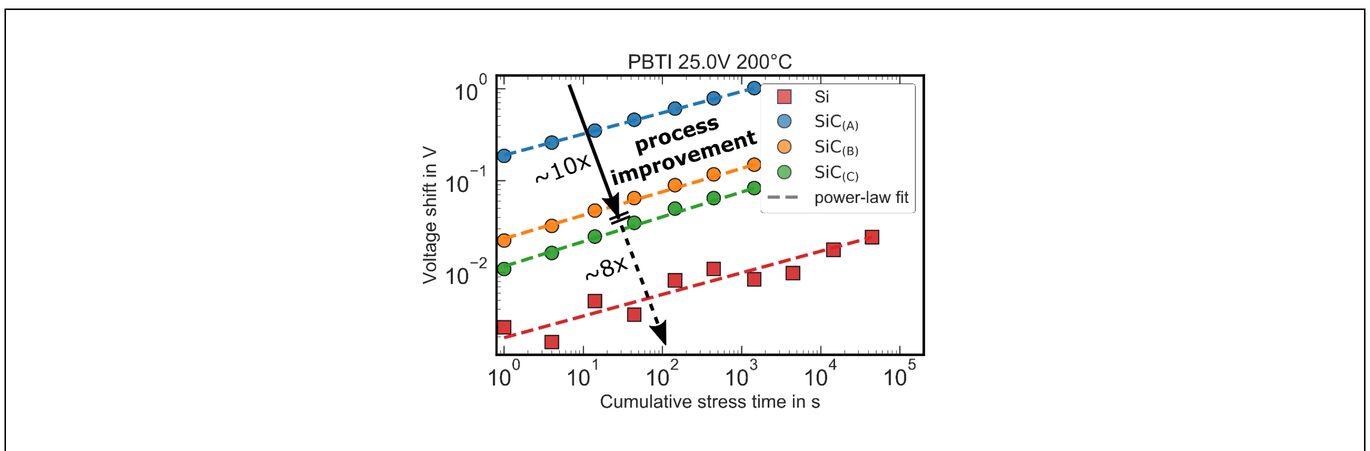

Figure 9 Time evolution of PBTI at 200°C using a stress bias of +25 V. Depending on the technology used and the device processing, the same time evolution but different absolute threshold voltage shifts are observed. PBTI is higher for SiC MOSFETs but still in the 100 mV range.

In fact, we observe the same change over time, voltage acceleration (Figure 10) and a similar temperature dependence of PBTI in SiC and Si power MOSFETs.

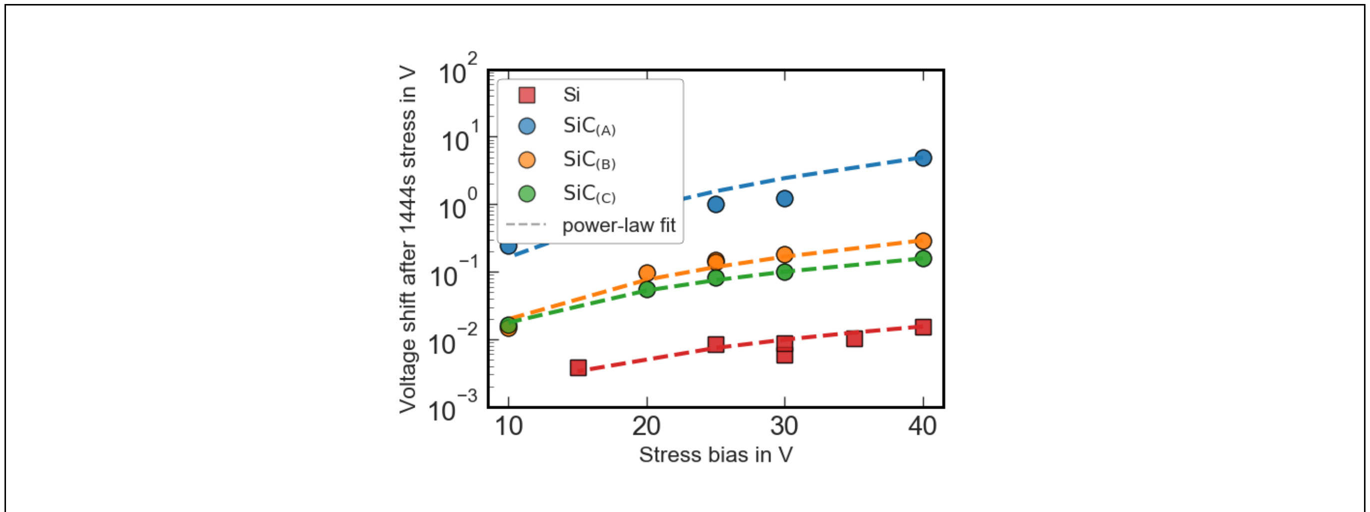

Figure 10 Voltage acceleration of PBTI at 200°C. All devices, regardless of SiC and Si technology, show the same voltage acceleration but different absolute drifts.

The remaining difference is an offset in the absolute threshold voltage shift. By optimizing device processing, we again achieved a drift reduction by one order of magnitude, thereby reaching drift levels in the 100 mV range within the experimental window of the test. Nevertheless, the best SiC devices still drift roughly 8 times more than the reference Si samples under these test conditions. For Si power MOSFETs PBTI is typically no issue at all. The observed offset in the drift is a natural consequence of the different band structure of SiC.

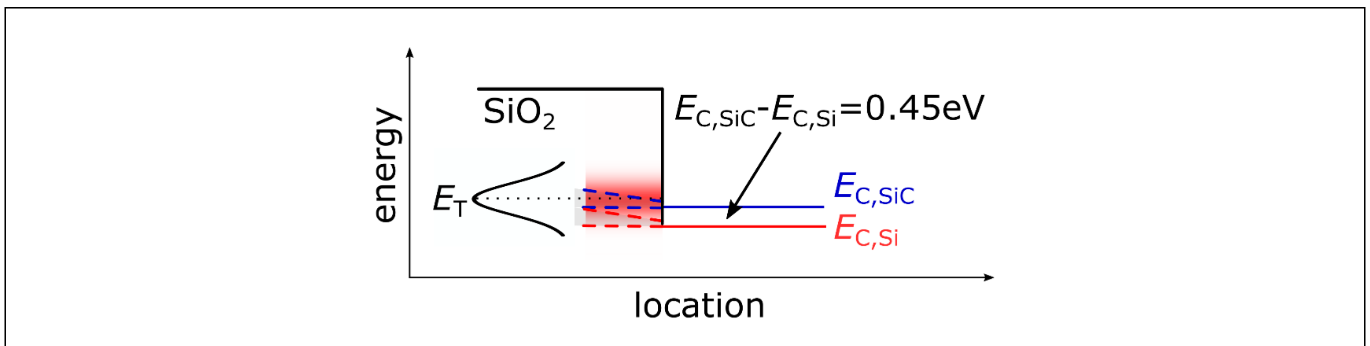

Figure 11 Band diagram of SiC/SiO_2 and Si/SiO_2 interfaces. In both technologies, the same trap distribution is present in the gate-oxide. Due to the higher conduction band minimum of SiC, this intrinsic trap level can be filled with less effort than in Si, leading naturally to higher PBTI drift in SiC even when assuming the same trap density in the SiO_2.

Figure 11 shows the band diagram for SiC/SiO_2 and Si/SiO_2 interfaces including a known intrinsic oxide trap level within the SiO_2 close to the conduction band edge of SiC [20]. As we demonstrated in [18], the higher conduction band minimum in SiC facilitates electron trapping into this trap level, which is the main reason for the larger drift of SiC devices after PBTI stress.

4.1.3.3 Drift modelling of DC BTI drift

Even though DC BTI has been studied extensively especially in Si technology, no commonly accepted physical drift model exists [17] [25]. Nevertheless, end-of-lifetime drift prediction is still possible using empirical models, such as e.g. an empirical power-law (cf. [26]) or Capture/Emission Time maps (CET maps, cf. [27]). Our studies revealed that the same predictive models developed and verified for Si technology (simple power-law and simple thermal activation model) are also very conveniently applicable to our SiC MOSFETs. Thus, DC BTI drift in SiC MOSFETs ends up to be as predictable as in Si technology.

4.1.3.4 Summary

DC BTI in SiC can be a serious reliability concern. Therefore, it needs to be minimized by optimized device processing and assessed carefully using appropriate measurement methods. However, a careful approach is needed since processing conditions, which yield better device performance (lower R_{ON} x A) are not always the best ones with respect to NBTI or PBTI. Infineon’s SiC MOSFETs show excellent device performance and at the same time very low NBTI, comparable to state-of-the-art Si power MOSFETs. The PBTI of SiC devices is somewhat higher compared to Si technology due to the larger band gap but still in the 100 mV range. The observation that PBTI in SiC shows similar dependence on time, temperature and bias points to the same underlying physics and allows the use of the same modelling approaches with the same prediction capability as with Si technology.

4.2 Parameter variations of SiC MOSFETs under real world application gate switching operating conditions (AC BTI)

4.2.1 Introduction

For years Infineon has been performing application relevant testing beyond standardized qualification procedures in order define reliable limits for safe operation in the final application [16] [18] [17] [19] [20]. The drift of threshold voltage and on-resistance under real world application operating conditions has been one “SiC-specific” focus of our intense research. We call the stressing of SiC MOSFETs under high frequency bipolar gate switching conditions and at elevated temperatures “AC bias temperature instability (BTI) testing”. Please note that this new “AC BTI testing” represent a major extension to the standardized “DC BTI tests”, which were discussed in the previous chapter and which are typically performed for Si and SiC MOSFET technology qualification. We decided to include these new type of stress tests into our standard qualification scheme for SiC MOSFETs since it turned out that under certain AC gate stressing conditions parameter drifts may exceed typical values observed after standard DC gate stressing. This is different compared to Si technology for which DC BTI has been considered always as “worst case” [28]. To create awareness about this new drift phenomenon and to provide design-in guidance to customers to avoid potentially critical operating conditions, Infineon has already published in 2018 an application note (AN) describing the basic features of AC BTI and has explained its

consequences in typical application environments [29]. In 2019 the AN was refined and extended to be consistent with latest findings. This white paper chapter is supposed to serve as supplemental material to Infineon's AN and provide a deeper insight into the dependencies of the AC BTI phenomenon.

4.2.2 AC BTI modelling

Extensive tests under various operation conditions were carried out by Infineon to develop a predictive semi-empirical model that describes the change in threshold voltage (V_{TH}) as a function of the relevant mission profile parameters experienced in typical SiC MOSFET applications such as stress time (t_S), gate bias low level (V_{GL}), gate bias high level (V_{GH}), switching frequency (f) and operation temperature (T)

$$\Delta V_{TH} = f(t_S, V_{GL}, V_{GH}, f, T, \ldots). \tag{1}$$

Measuring threshold voltage while switching the MOSFET at high frequencies (e.g. 500 kHz) is particularly challenging since it requires high resolution of electrical parameters and at the same time measurement time delays in the microsecond range. For this purpose Infineon has developed custom-designed high-end stress/test equipment allowing for fast in-situ parameter monitoring during AC gate stressing [16].

One characteristic of AC BTI is that the drift in threshold voltage is always positive for all parts we have investigated. An increased threshold voltage reduces the MOS channel overdrive (V_{GH} - V_{TH}) and therefore increases the channel resistance (R_{ch}) of the device

$$\boldsymbol{R_{ch}} = \frac{\boldsymbol{L}}{\boldsymbol{W \mu_n C_{ox} (V_{GH} - V_{TH})}}. \tag{2}$$

In equation (2) L is the length of the channel, W is the width of the channel, μ_n is the free electron mobility, C_{ox} is the gate oxide capacitance, V_{GH} is the gate voltage high level and V_{TH} is the threshold voltage of the device. In high power devices, the channel resistance is only one component of the total on-resistance of the device

$$R_{ON} = R_{ch} + R_{JFET} + R_{epi} + R_{sub}. \tag{3}$$

In equation (3) R_{ch} is the channel resistance, R_{JFET} is the junction-field-effect-transistor (JFET) resistance and R_{epi} is the epitaxial layer resistance of the drift region, and R_{Sub} is the resistance of the highly doped SiC substrate. An increased channel resistance (ΔR_{ch}) due to a reduction in gate overdrive (ΔV_{TH}) eventually leads to a slight increase in the total on-resistance of the device (ΔR_{ON}). This increase may lead to higher static losses, and thus, to a slightly elevated junction temperature during operation. To prevent operation conditions which could cause a potentially critical drift in on-resistance (> 15%, already considered in the datasheet with the maximum ratings) during continuous switching operation for 10 years at 125°C, Infineon's AN provides guideline-charts for recommended gate drive voltages and

frequencies. The basis of these guideline-charts is the degradation model that was created after intensive studies and measurements of the basic characteristics of AC BTI.

4.2.3 Basic characteristics of AC BTI

This paragraph illustrates a collection of experimental data revealing the basic characteristics of AC BTI. The drift model was fitted to the data to derive the semi-empiric model coefficients. The shown fit lines correspond to the drift model used for calculating the gate voltage guideline charts in the AN [29].

4.2.3.1 Dependence on switching frequency (f)

AC BTI depends on the number of switching events and the AC VTH drift follows a power-law:

$$\Delta V_{TH_AC} \sim (t_s \times f)^n \quad (4)$$

Therefore, it is more appropriate to plot the AC drift as a function of the number of switching events instead of plotting drift versus stress-time as typically done for DC BTI. In Figure 12 we compare two different switching frequencies. The drift seen at the same number of switching events is similar if not identical and independent of the total stress time. That is the reason why applications running at higher switching frequencies (e.g. solar) are more affected by AC BTI as compared to applications that run at comparatively lower switching frequencies (e.g. drives). In addition, since the static losses are predominantly affected, the final impact of the AC BTI drift on the total losses in the application depends on the given ratio between conduction and switching losses. In a given application if the switching losses are the dominant portion of the total losses then even if the switching frequency is higher any increases in the conduction losses might not be critical for the system design.

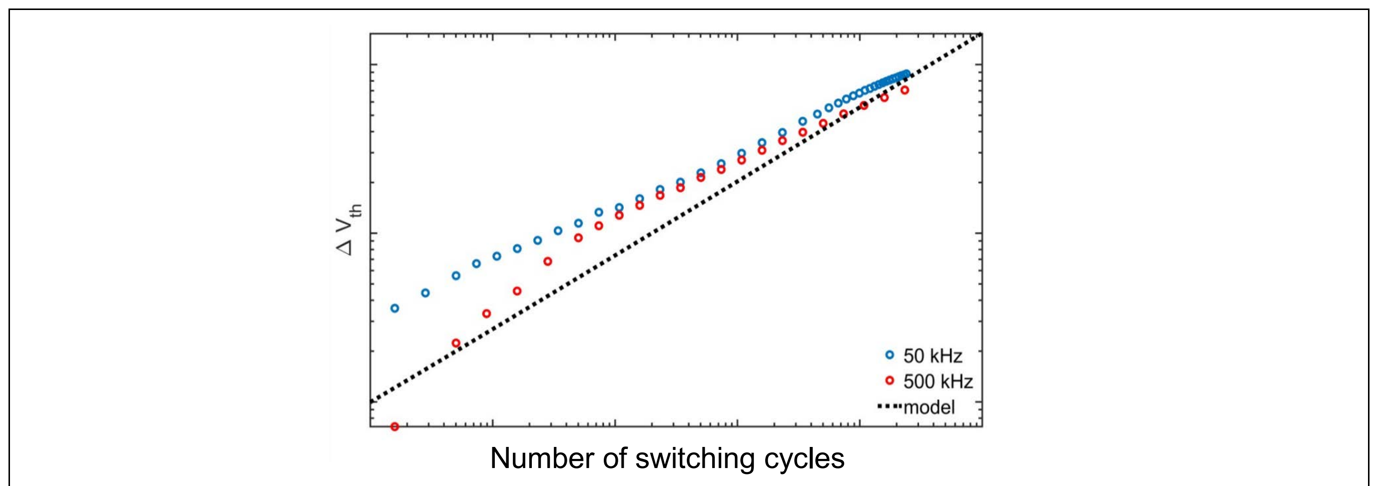

Figure 12 AC VTH drift measured under accelerated gate voltage (V_{GH} > 18V; V_{GL} < -5 V) and temperature (T_S > 150°C) conditions. Data was recorded using the same total stress time but different stress frequencies (50 and 500 kHz). The AC VTH drift shows a power law-like increase proportional to the number of switching cycles. The drift model is indicated as dashed line.

4.2.3.2 Dependence on gate bias low level (V_{GL})

Another unique characteristic of AC BTI is its dependence on the gate bias low level (V_{GL}). In fact, AC BTI only leads to enhanced V_{TH} drift if SiC MOSFETs are operated for a long time in a mode when a negative gate bias is applied in off-state. If devices are switched-off at V_{GL}= 0 V, the obtained V_{TH} drift shows the typical DC BTI drift behavior without being dependent on the number of switching events or cycles. A large negative gate voltage in off-state affects the V_{TH} drift in the following way (c.f. Figure 13): at low numbers of switching cycles less V_{TH} drift is seen due to relaxation effects, however, at high numbers of switching cycles the drift is typically higher for more negative off-state gate voltages due to a larger drift slope (power-law exponent).

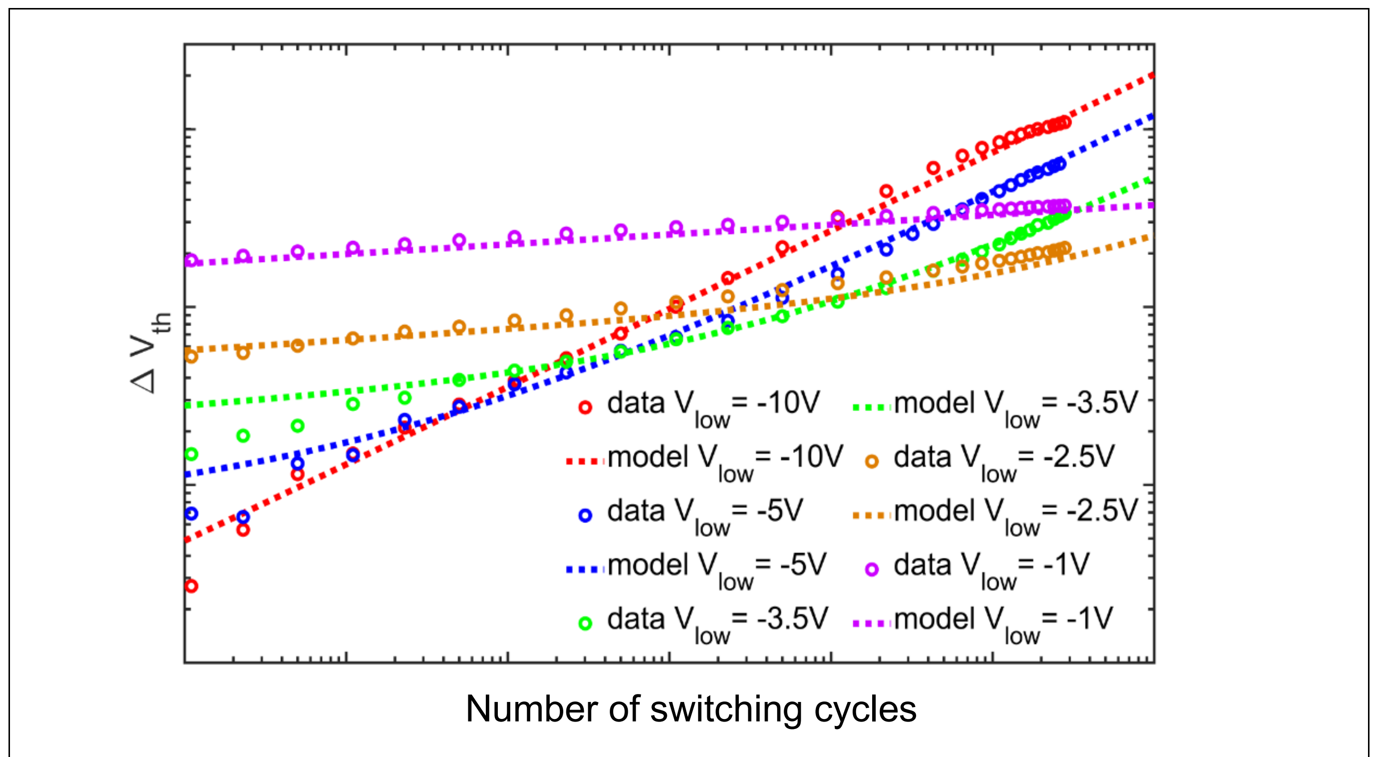

Figure 13 AC VTH drift measured under accelerated conditions by using a high number of pulses in a short time (f = 500 kHz), gate voltage high level (V_{GH} > +18 V) and temperature (T_S > 150°C) conditions. Data was recorded using different gate voltage low levels. Using gate voltage low levels higher than -2.5 V, e.g. -1 V, the amplitude and slope of the V_{TH} drift is similar or lower compared to DC BTI. When stressing at more negative gate voltage low levels, e.g. -5 V, AC BTI starts to become dominant after a large number of switching periods. This is due to a steeper drift slope (power-law exponent) of AC BTI. The drift model (dashed-lines) fits very well to the measured data.

4.2.3.3 Dependence on gate bias high level (V_{GH}) and temperature (T)

AC BTI depends in a similar way as DC BTI on the gate voltage in on-state (V_{GH}) and on the operating temperature (T). Larger V_{TH} drift values are observed at higher V_{GH} levels and at elevated temperatures as shown in Figure 14 and Figure 15. However, this does not automatically mean that such operating conditions are more critical for the application.

At higher V_{GH} levels one observes a larger BTI. On the other hand, the total on-resistance becomes less sensitive to V_{TH} variations due to the increased gate overdrive. As a consequence, the relative change in R_{ON} at higher V_{GH} values may be even lower despite of a higher V_{TH} drift. This yields, for instance, more relaxed curves for operation with an 18 V on state voltage compared to a 15 V on state voltage.

Elevated temperatures typically also lead to larger BTI. On the other hand, at elevated temperatures JFET and drift zone (epi) resistances become more pronounced with respect to channel resistance. As a consequence, the relative change in R_{ON} at higher temperatures may again be lower despite of a higher V_{TH} drift.

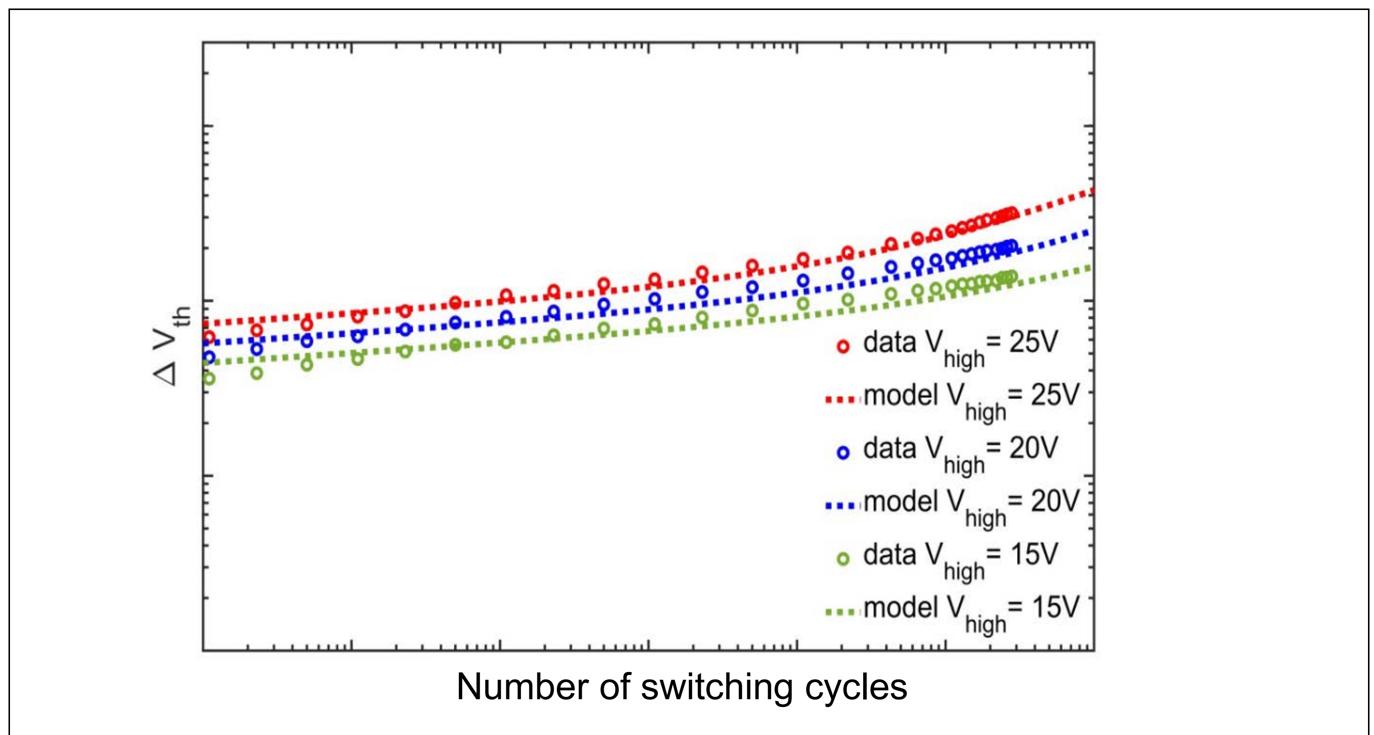

Figure 14 AC VTH drift measured under accelerated frequency (f = 500 kHz) and temperature (T_S > 150°C) conditions. Data was recorded using a typical gate voltage low level and different gate voltage high levels. Stressing with larger gate voltage high levels leads to a nearly parallel shift of the measured data. The drift model (dashed-lines) fits very well to the measured data.

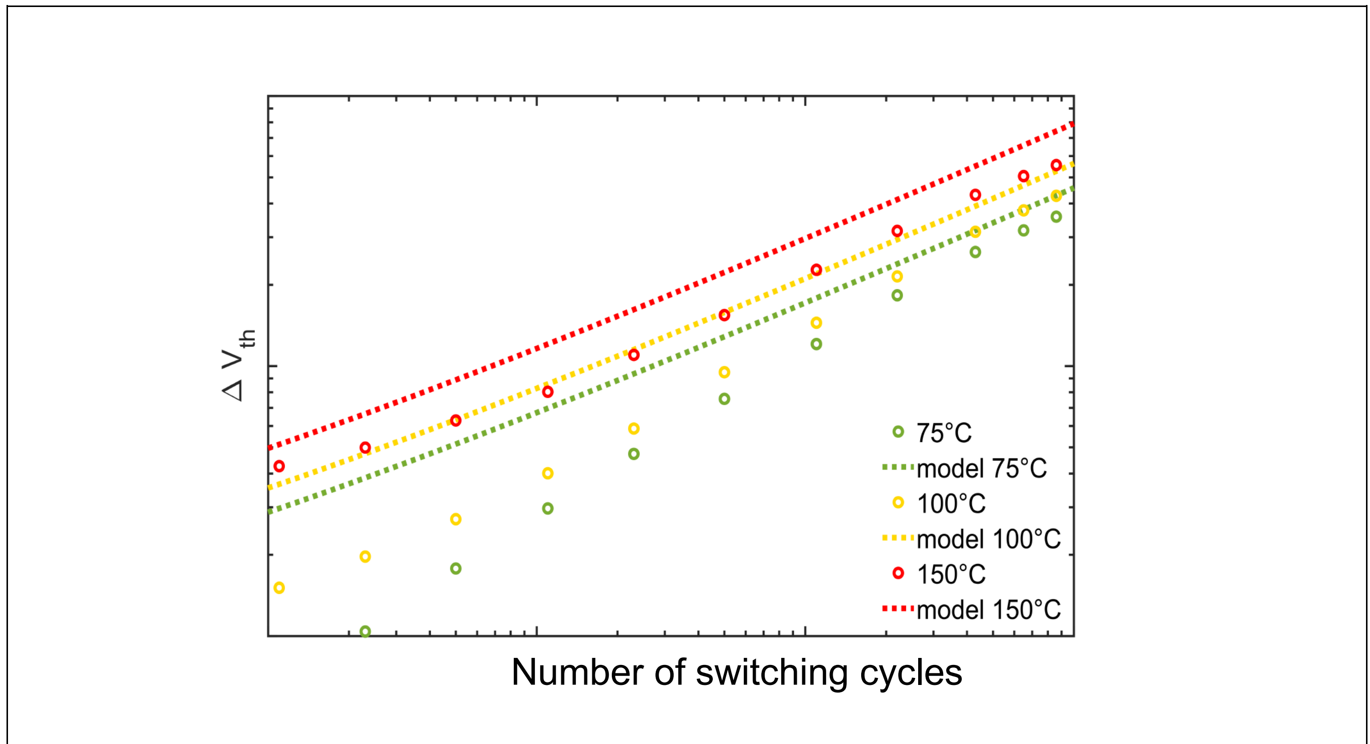

Figure 15 AC V_{TH} drift measured under accelerated frequency (f = 500 kHz) and gate voltage high level. (V_{GH} > 18 V) conditions. Data was recorded using a typical gate voltage low level and different stress temperatures. Stressing at higher temperature leads to a parallel shift of the measured data. The drift model (dashed-lines) fits the trend of the measured data but slightly overestimates the absolute value of the drift in this experiment.

4.2.3.4 Drift saturation

We have performed switching frequency accelerated AC gate stress experiments for nearly 1 year to study long-term AC BTI under typical application switching conditions. The drift observed in these long term experiments suggests that the actually measured AC BTI drift at the end of life can be lower than the drift predicted by the drift model, as the effect starts to saturate.

4.2.3.5 Dependence on load current

To complete the assessment several experiments with various load currents have been executed. The observed V_{TH} and R_{ON} drifts basically follow the AC BTI drift model suggesting that the load current itself does not alter the observed drift behavior. It was, however, found that over- and undershoots in the gate signal, which may naturally occur in inverter applications, may affect AC BTI. This has been pointed out in the second version of Infineon's app-note and particular guidelines were given how to correctly assess and suppress over- and undershoots in the application.

5 Silicon carbide cosmic ray robustness

Semiconductor devices are subject to nuclear particle irradiation during their whole lifetime. This irradiation originates from high energy cosmic particles hitting the outer periphery of the atmosphere and by propagation and nuclear reactions creating a shower of nuclear particles at lower altitudes, see Figure 16.

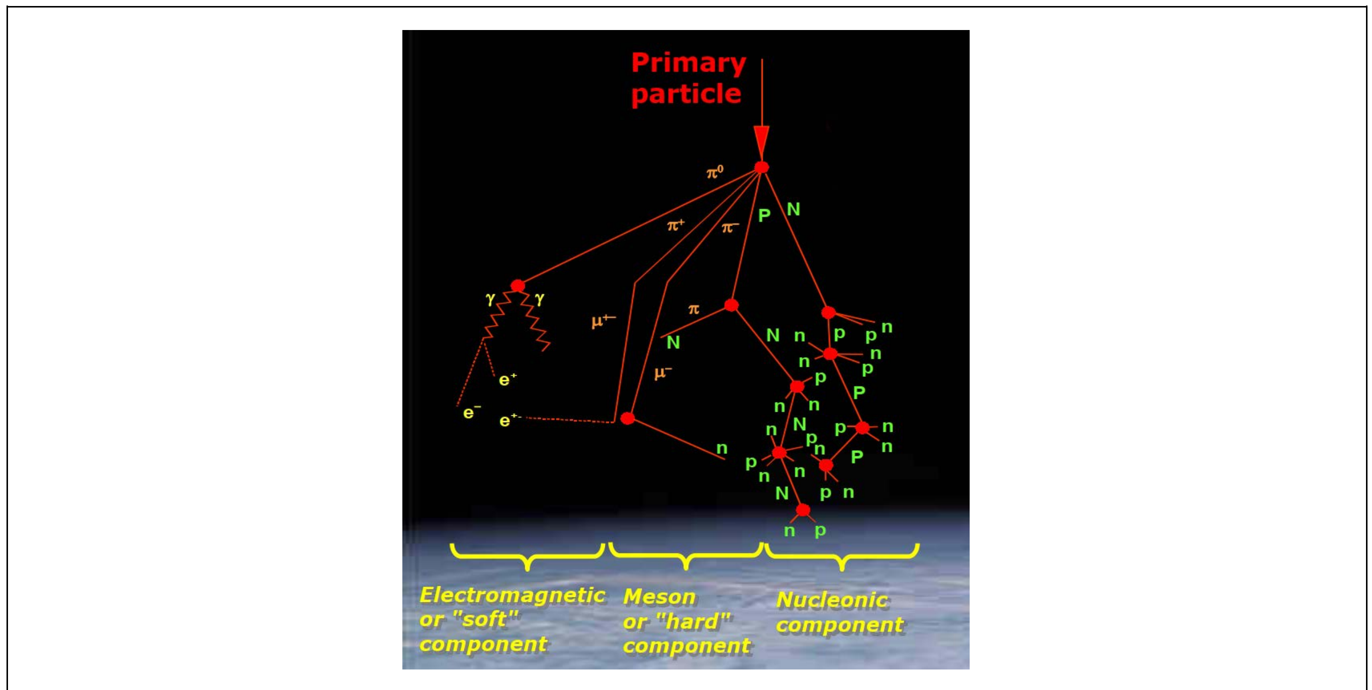

Figure 16 Schematic of a cosmic particle induced particle shower after [12].

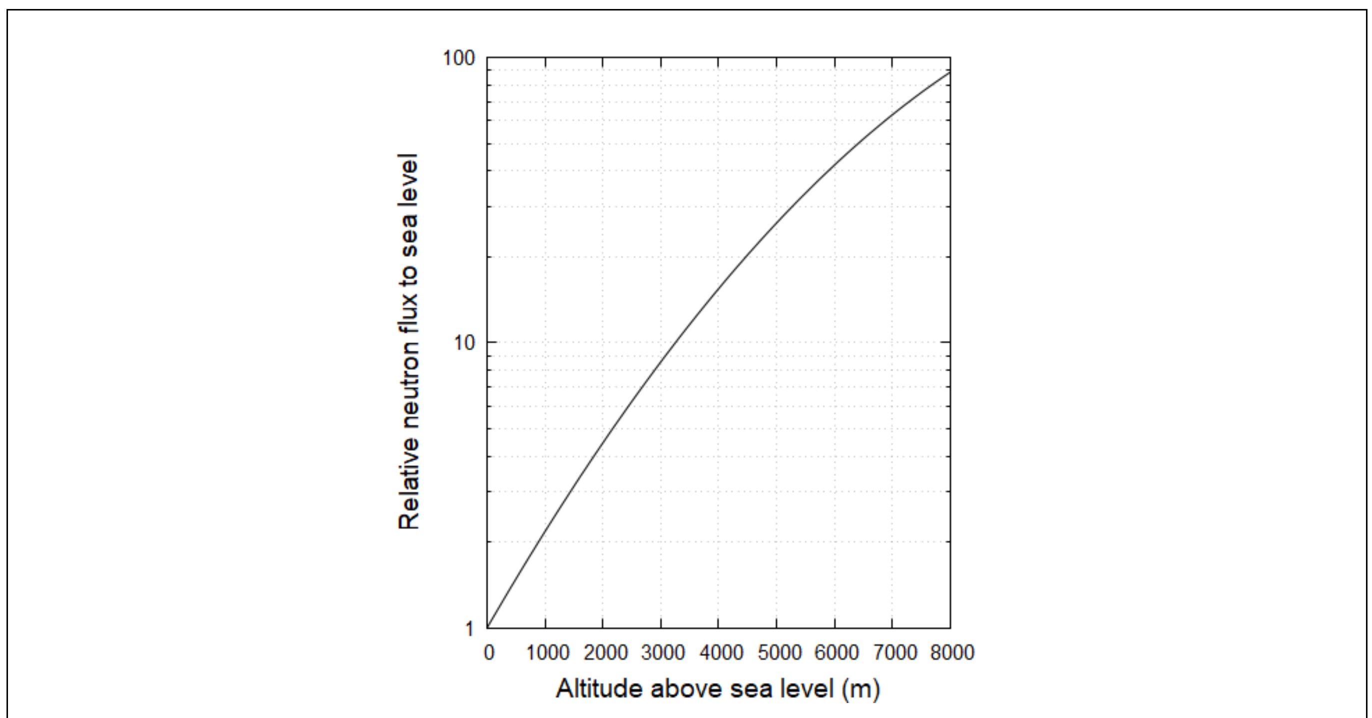

Figure 17 Relative neutron flux compared to sea level at elevated altitudes [13].

For space applications above the earth's atmosphere cosmic radiation largely consists of protons, ions and gamma rays. For terrestrial applications, up to aircraft altitudes, the atmosphere provides a high level of shielding and the radiation environment is governed by neutrons with a flux density of about 20 neutrons per cm^2 an hour [13] at ground level. However, as depicted in Figure 17, the neutron flux increases exponentially with altitude [14] and therefore altitude has to be taken into account when considering cosmic radiation induced failure rates.

Despite the rather low terrestrial neutron flux density, many power semiconductor applications have a requirement for single device failure rates in the range of 1 – 100 Failures In Time FIT or even lower. (1 FIT = 1 failure in 10^9 hours of operation) It is therefore necessary to identify and understand the cosmic radiation induced failure mechanism of power semiconductor devices and to derive an acceleration model depending on device and application parameters, see also [20].

Figure 18 shows the basic failure mechanism for a power semiconductor device operating in a blocking or reverse biased condition. The sketch depicts the electric field distribution in a blocking p-i-n diode structure. An incident cosmic particle may trigger a nuclear reaction with a lattice atom and the recoil ions initiate a charge plasma of electrons and holes. In normal reverse biased operation, the electric field exhibits a triangular or trapezoidal shape (blue curve). In the presence of a charge plasma induced by an incident cosmic particle, the E-field is screened locally within the plasma. At the edges of the plasma region even higher electric fields occur which may lead to an avalanche generation propagating further through the active region (red curve), a so-called streamer.

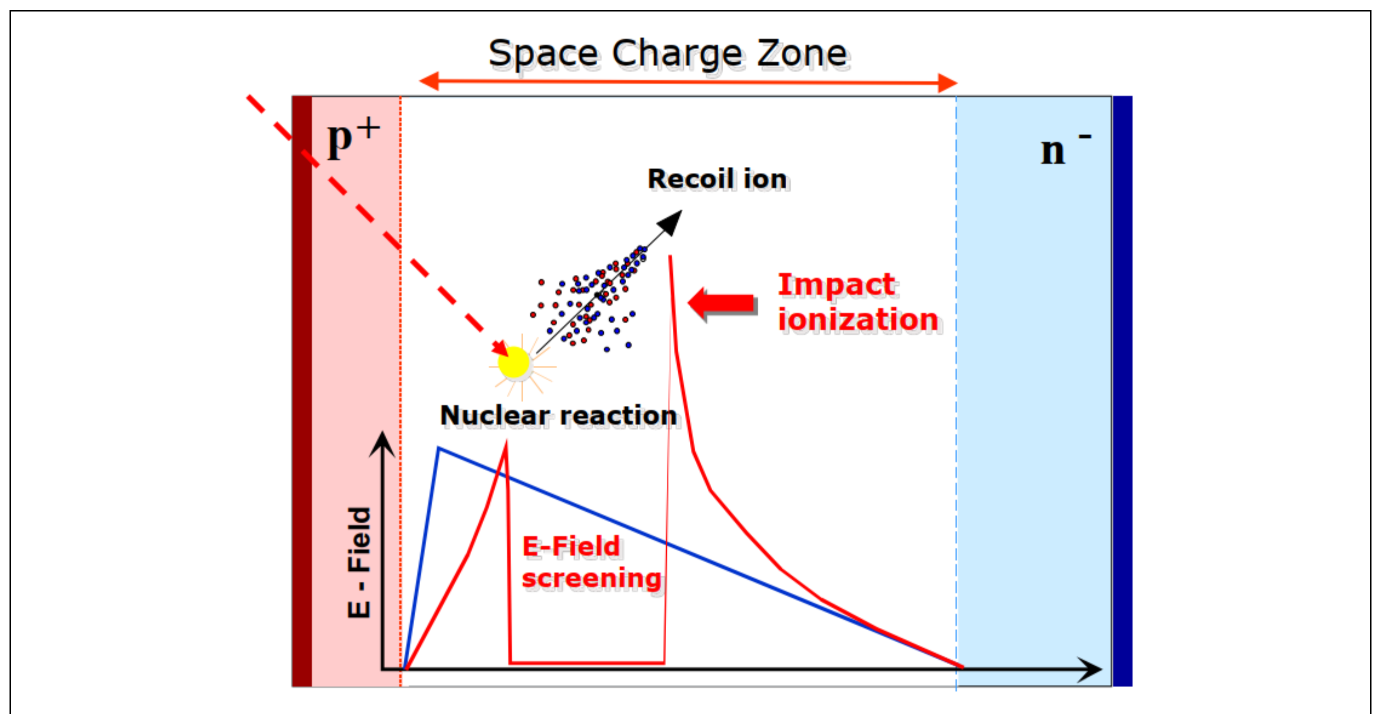

Figure 18 Schematic of a cosmic radiation failure mechanism in a vertical power device after [12]. For simplicity, a one dimensional p-i-n diode structure with applied reverse bias is considered.

The plasma channel and the subsequent streamer effectively short out the device, which is then destroyed by the dissipated energy. This is called a Single Event Burnout (SEB). In Silicon carbide as well as in Silicon the cosmic radiation induced failure rate increases exponentially with the electric field present in the device at the incident moment. Devices with similar electric field show similar failure rates. Within the past decades numerous accelerated experiments have been performed which show a similar cosmic ray failure rate if the applied voltage is normalized to the actual avalanche breakdown voltage, see Figure 19 and [16].

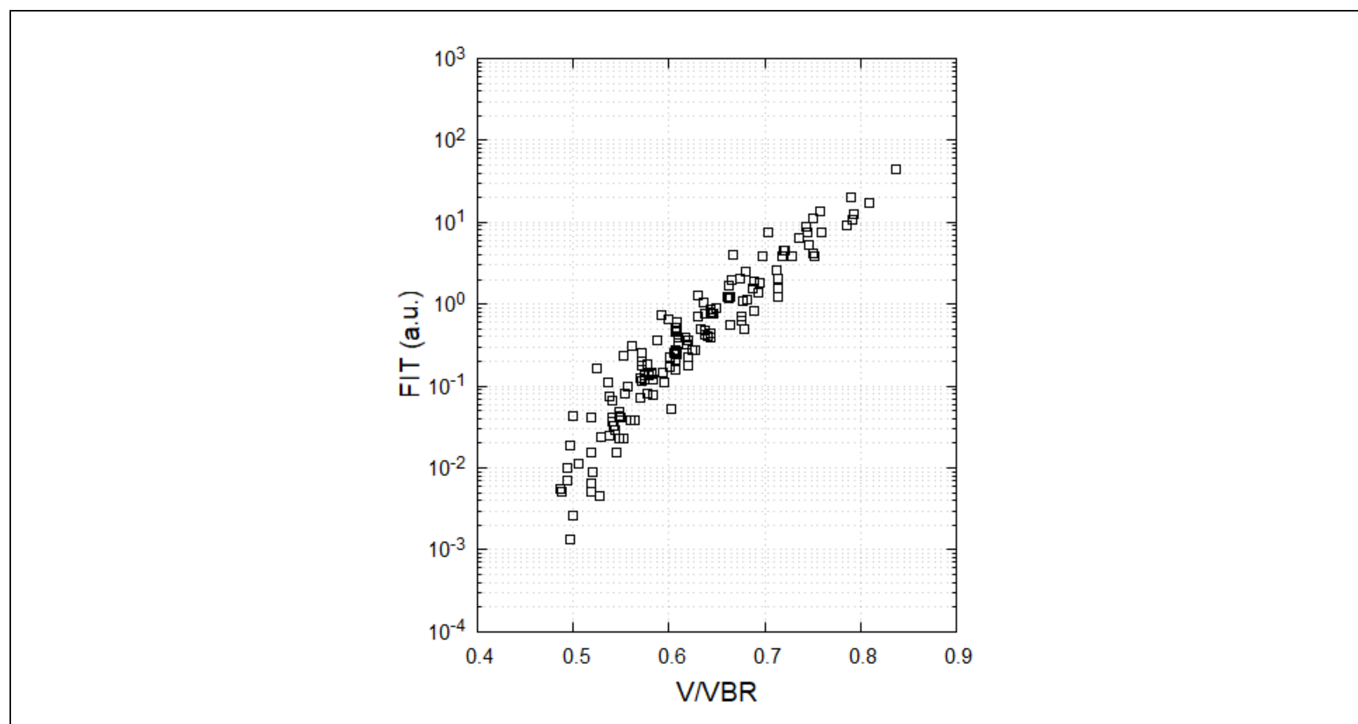

Figure 19 Measured FIT rate of numerous experiments of different SiC technologies and voltage classes. The voltage of each experiment is normalized to the measured actual avalanche breakdown voltage V_{BR}. A similar result is reported in [16]. Due to the – in principle – low failure probability and the high acceleration in the experiment, the experimental results exhibit a rather large scatter in the range of 1 to 2 orders of magnitude. The statistical error bars of each single experiment stemming from the limited number of devices in the test are not shown in this plot for simplicity.

These experiments are carried out with proton accelerators and spallation neutron sources, which allow for a high acceleration factor in the order of 10^8 by means of a high particle flux density [13]. Figure 19 shows a clear exponential dependence of the failure rate on the applied reverse or blocking voltage. Due to the in principle low failure probability per device and the limited statistics in the experiments the results show a scatter in the range of 1-2 orders of magnitude. Apart from this scatter, one can derive an average exponential voltage acceleration model from these results. Accelerated tests with artificial sources are accompanied by storage tests under the natural flux of atmospheric neutrons at high altitudes in order to verify the acceleration model [15].

By the dependency of cosmic ray failure rate on avalanche breakdown voltage, it is possible to tune the robustness of power devices. Generally, vertical power devices can be designed for a higher avalanche breakdown voltage, and thus increased cosmic radiation robustness, by larger thickness and lower doping of the drift or base layer. This in turn implies a certain degradation of the forward conduction losses, i.e. there is a trade-off between radiation robustness and on-state losses.

To calculate the cosmic radiation failure rate of devices or modules, the mission profile of the specific application, i.e. applied voltage and altitude vs. respective operating hours has to be considered. Therefore, it is not possible to provide a single number of cosmic radiation failure rate for a certain technology or application. Instead, Infineon supports their customers via its worldwide network of experienced application engineers who have been trained on how to calculate overall failure rates based on Infineon test data, the customer mission profile and application details.

Infineon is permanently supporting the development of new technologies and products with cosmic radiation experiments to verify the model and to ensure the radiation robustness needed in the application and the device design for the proper trade-offs. It can be shown that there are only minor differences between the silicon IGBT technology and SiC power devices with respect to the cosmic ray basic failure mechanism and its dependency on operating conditions.

6 Short circuit ruggedness of CoolSiC™ MOSFETs

While a typical industrial IGBT is designed today to handle around 10 µs short circuit time, SiC MOSFETs show none or just a few µs short circuit capability. Often this is misinterpreted as a fundamental deficiency of SiC MOSFETs. However, a much more detailed analysis of the background shows that even certain IGBT types exist which cannot handle short circuits (e.g. designed for soft switching applications) and that certain cell design measures in SiC MOSFETs can extend the short circuit performance to values known for typical IGBT's as well. Taking into account that the major target applications for SiC MOSFETs today do not require a short circuit handling capability (or even just the mentioned few µs) it can be concluded that this deficiency is at present of minor importance. Furthermore, it has to be pointed out that an increase in the short circuit capability will have a large negative impact on $R_{DS(on)}$. Thus, the decision to add short circuit ruggedness in form of a guaranteed short circuit withstand time should be carefully considered. If it is decided to specify this in the data sheet it is mandatory to implement measures to ensure the performance of production parts. At Infineon, this is done with a 100% production test on all products before shipment. There is a common request from customers to specify the number of short circuit events that a part can survive in the application. This question cannot be easily answered since the actual conditions for short circuits (stray inductance etc.) can vary a lot under different operating conditions. In this case a specific assessment between supplier and end user is the only way to address the question.

The following chapter should serve to explain the background for the difference between IGBTs and SiC MOSFETs starting with a brief review of the actual short circuit destruction mechanisms. In a typical short circuit event the full (DC-link) voltage is applied to the device accompanied by a current defined by the load impedance and the output characteristic of the semiconductor. So a simultaneous high voltage and current leads to a very high power loss and thermal stress in the device. As expected the thermal destruction is the key limiting factor, actual melting of metal layers is one observed failure mode. The time duration is in the range of microseconds. In case of SiC various other findings are reported, e.g. gate shorts after a successfully passed short circuit event [22]. A failure like it is sometimes observed for IGBTs, based on a too high leakage current after the stress pulse, which then leads to thermal runaway subsequent to the short circuit pulse. However this type of failure mode, can be ruled out based on the existing experience and knowledge of SiC devices.

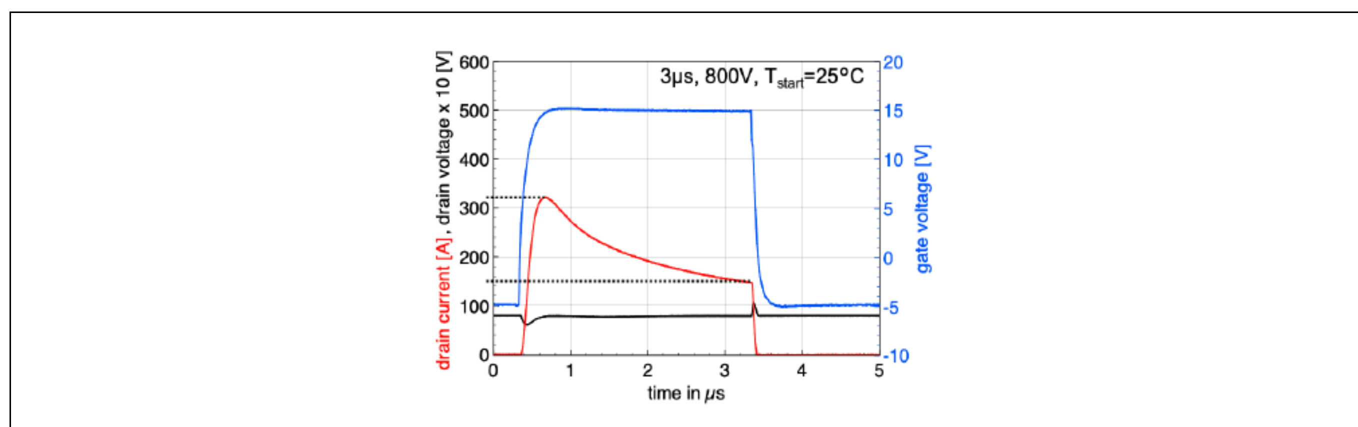

Figure 20 Typical short circuit waveforms for a SiC MOSFET with 45 mΩ and a nominal DC current rating of 20 A.

Another important observation is that under short circuit the temperatures within the chip are substantially higher and have a different distribution compared to IGBTs. Higher temperatures occur because also the peak currents are substantially higher, as a ratio of the device rated current, than for IGBTs which benefit from saturation effects. While MOSFETs are designed to have a very low $R_{DS(on)}$ achieved by using short channels and a limited JFET effect. The result is that the SiC MOSFET peak current can be about 10X the nominal device current, with an IGBT this value might be only 4 x the nominal current, immediately after the short circuit starts (see Figure 20). Even though later the current drops down to a value which can be turned off safely (see dashed line in Figure 20), again the overall temperature can still rise.

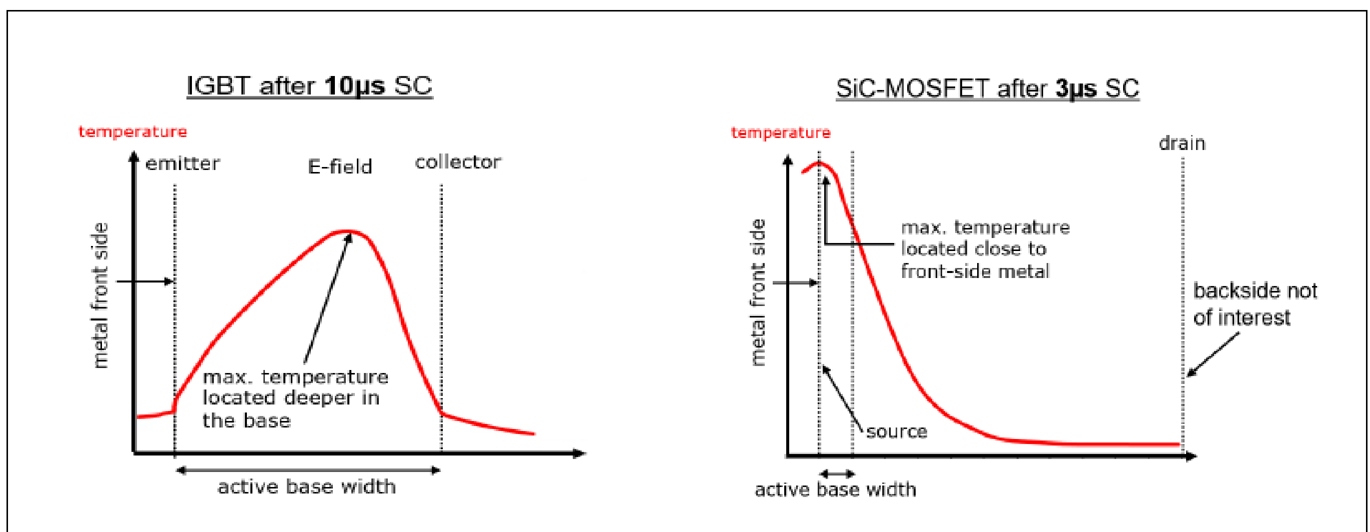

Figure 21 Schematic temperature distribution after short-circuit event of an IGBT (left picture) and a SiC MOSFET (right picture).

For a SiC MOSFET as the short circuit time and resulting power loss are in the range of 2–3 µs the entire chip heat capacity cannot be utilized and the heat is generated almost completely in the very thin drift zone that is close to the surface of the chip and isolating oxide layer and top layer metallization. Figure 21 depicts this situation and compares it to an IGBT. In the high voltage silicon device the peak temperature has a lower amplitude and is located more in the bulk of the device. Thus, different failure modes will occur and so for the SiC MOSFET other mitigation measures are in place to adjust the short circuit behavior of the device.

Infineon’s CoolSiC™ MOSFET products are specified today with up to 3 µs short circuit withstand time and the specified value is tested 100% on packaged level before shipment.

For SiC MOSFETs it is important to reduce the peak current under short circuit. This can be achieved by a more pronounced JFET effect of the p-body regions or a reduced V_{GS}. Further ideas as presented in [23], exist. However, all of them have a negative impact on the on-resistance. Thus, a deep understanding of the system requirements and behavior is needed to derive potential device related measures and system innovations [24] to deal with short circuit events while maintaining the extraordinary performance of SiC under nominal operating conditions.

7 SiC body diode bipolar degradation

7.1 Mechanism

The bipolar degradation effect can appear in any type of SiC devices under bipolar operation (PN junction, e.g. the body diode of a MOSFET, when conducting current). The effect is primarily triggered from pre-existing basal plane dislocations (BPDs) on the SiC crystal. During the bipolar operation, the energy released by the recombination of electrons and holes causes stacking faults to expand at BPD's [25]. The stacking faults will grow to the surface of the chip and then stop growing. Areas covered by the grown stacking fault as shown in Figure 22 on the left side cannot conduct current any longer, therefore the effective active area of a chip is reduced.

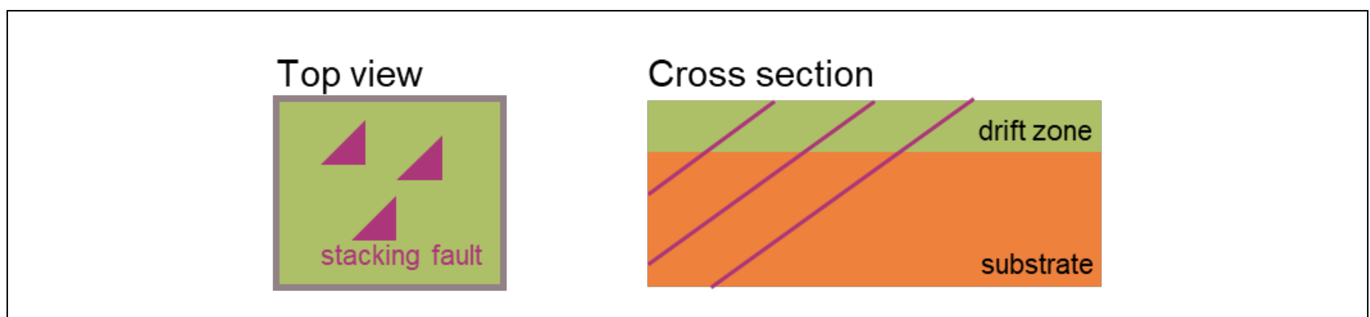

Figure 22 Top view and cross section of stacking fault in a SiC devices

Based on the underlying physical background, it can be concluded that the bipolar degradation is:

- **A mechanism with a certain probability to occur or not.** For the devices without BPDs (or BPD's not subjected to recombination events), there will be no bipolar degradation effects.
- **Common effect to all SiC devices.** Since the BPDs are a common defect in a SiC substrate (wafer), the bipolar degradation could happen to any SiC devices with PN junction regardless of device type and manufacturer.
- **A saturating effect.** Once the stacking fault reaches to the surface of the device, the bipolar degradation will saturate. Depending on operating condition, e.g. the current through the PN junction and the junction temperature, the time from initial state to saturation could be from several minutes to hours of accumulated bipolar operation time.

7.2 Effects in the application

As mentioned before, the area with grown stacking faults inside appears to show a higher resistance, therefore reducing the current flowing through it. Figure 23 shows a thermal image (EMMI) of SiC devices with and without defects. It can be clearly seen that the areas with stacking faults have almost no heat generated in them due to very low current levels.

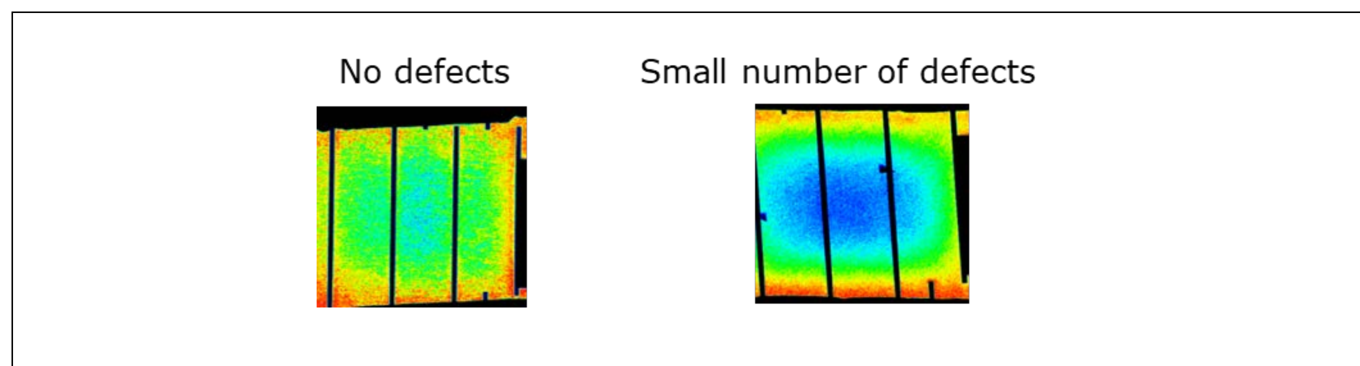

Figure 23 EMMI image of a SiC MOSFET under conduction mode with a small number of defects (small dark triangle, see arrow) and without defects. Colors indicate current densities (blue low, red high), the bold black line are inactive device regions.

From experiments, it can be confirmed that the bipolar degradation only reduces the active area of SiC devices, meaning, for MOSFETs the $R_{DS(on)}$ and for the body diode the V_{SD} increases. Other essential parameters, e.g. breakdown voltage, switching behaviors and as well the oxide reliability of the devices, do not change.

Therefore, if a SiC device with a small number of defects and after saturation of the $R_{DS(on)}$ or V_{SD} increase still stays within the datasheet margins and there will be no long term negative effect in operation.

7.3 CoolSiC™ MOSFET – strategy to eliminate the risk

Infineon has dedicated measures in place to ensure stable performance of its products delivered to the customers. Two measures have been applied to ensure that all CoolSiC™ MOSFETs with the possibility of using the body diode are shipped **without** any bipolar degradation leading to data sheet violation.

This includes an optimized chip production process in order to suppress stacking fault formation, combined with effective verification measures.

8 Qualification at the product level

8.1 Testing beyond today’s standards according to real world mission profiles

For both discretes and modules regular tests according to relevant standards are applied, namely HTRB, H3TRB and HTGS. These tests are mandatory for the release of the technology and the results are documented in the PQR’s (Product Qualification Reports) available on the web for each product.

To ensure reliable function of our new CoolSiC™ MOSFET beyond these standards, all standardized tests have been performed once for at least 3000 h to check the robustness of our new technology far beyond the necessary standard conditions. Systematic EoL mechanisms could not be identified in any of these tests, showing the high degree of reliability of our CoolSiC™ MOSFETs.

In recent years there has been a shift for many applications to require a humidity robustness beyond the standard H3TRB conditions. Measures at chip level are needed protect power devices against moisture related degradation and tests have to be designed to verify the effectivity of such measures in an accelerated way. From IGBT modules, different degradation mechanisms under those conditions, like metal corrosion or dendrite formation, are known [39]. During a standard H3TRB qualification, robustness against these failure mechanisms is ensured at T = 85°C and a relative humidity rH = 85% and V_{DS} = 80 V according to [40]. As described, these test conditions are not enough to ensure long term reliability for all applications. If the analysis of the application profile reveals extreme harsh conditions, additional tests have to be done. Nowadays moisture tests under 80% of maximum drain source Voltage are used (HV-H3TRB) to ensure long term reliable operation of the devices [39]. For IGBT modules literature states that such tests done for 1000 h are enough to ensure up to 25 years of lifetime [39].

As the dimensions of the edge terminations of SiC devices are shrunk, because of the higher blocking capability of the material, it is important to use special passivation concepts robust enough to withstand not only the extreme conditions applied in these tests but also operation in the real application. To verify a reliable function of our SiC chips during the full operating lifetime, H3TRB and HV-H3TRB were performed during the qualification of our CoolSiC™ MOSFETs. Degradation mechanisms could not be identified either in the H3TRB or in the much more challenging HV-H3TRB tests. For example, I-V curves before and after the HV-H3TRB test are shown in Figure 24. None of the stressed systems shows an increased leakage current of more than single digit µA. This is also visible in the leakage current monitoring displayed on the right side of Figure 24, normally also used as indicator for the beginning of degradation [39]. As the leakage currents are not increasing under stress, it is clear that the devices are showing no signs of starting to degrade under stress. To identify potential new failure mechanisms for our SiC devices, tests with a large statistical sample of 300 chips were performed lasting up to 3000 h without discovering systematic EoL mechanisms. This is equivalent to more than 75 years of secure field operation if the values given in literature for Si chips are extrapolated [39].

In addition, we also tested our devices under Pulsed High Voltage humidity conditions (PHV-H3TRB or dynamic HTRB) without discovering signs of degradation. As the HV-H3TRB is regarded as the more challenging test because of the higher permanent voltage, the PHV-H3TRB is not necessary for release.

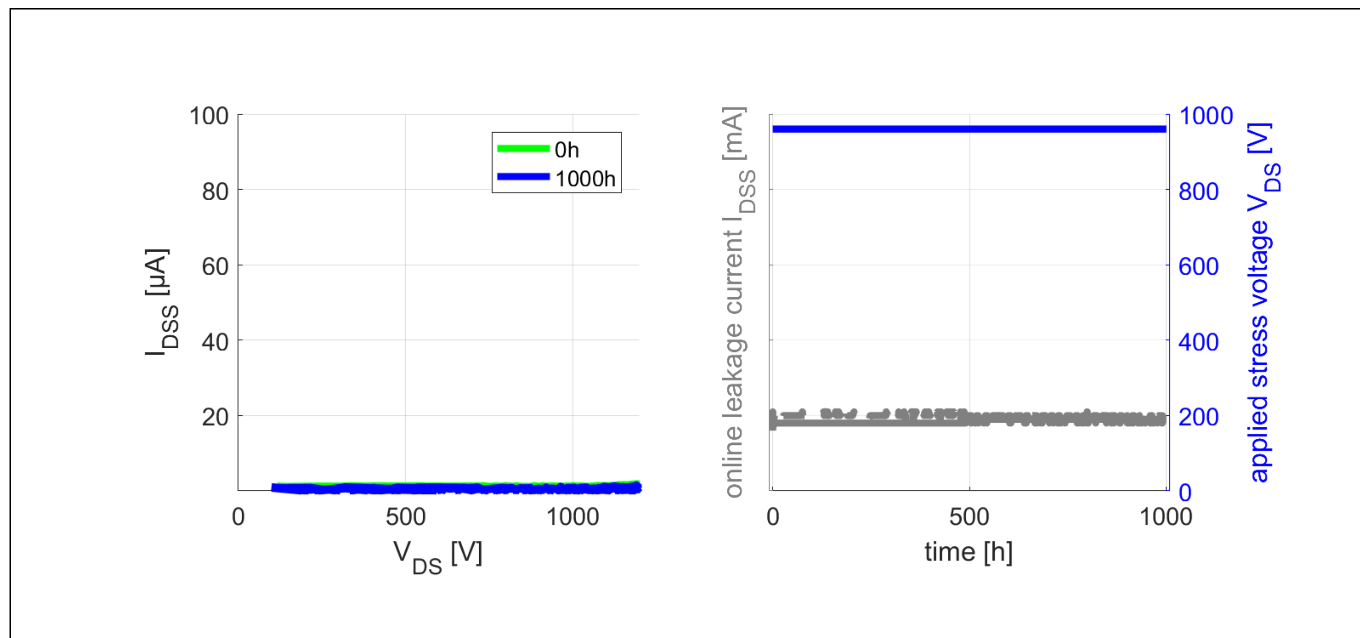

Figure 24 On the left side, leakage currents before (blue) and after stress (green), are shown. The right side displays the leakage currents measured during stress

Table 1 summarizes all the long-term reliability tests conducted for power modules at Infineon incorporating SiC MOSFETs. By performing these tests even for extended times, Infineon has proven that there are no unknown failure modes for our new CoolSiC™ MOSFET triggered under the test conditions shown in Table 1. To secure reliable operation under field conditions, the qualification stress times combined with strict pass/fail criteria are sufficient.

Table 1 Chip storage tests performed with 1200 V rated CoolSiC™ MOSFET in modules. The additional robustness validation stress time is also given, a systematic end of life mechanism could not be found during any of these tests.

Test	Test conditions	Qualification stress time	Robustness validation beyond standard
HTRB	V_{DS} = 1080 V, T_{vj} = 150°C	1000 h	+4000 h
HTGS	V_{DS} = 0 V, V_{GS} = +20/-20 V, T_{vj} = 150°C	1000 h	+4000 h
H3TRB	V_{DS} = 80 V (100 V for AEC), T_a = 85°C, rH = 85%	1000 h	+2000 h
HV-H3TRB	V_{DS} = 960 V, T_a = 85°C, rH = 85%	1000 h	+2000 h

For reliability tests performed with discrete devices, the high operating temperature or mold compound might have an additional impact on the long-term stability of the device under stress. Therefore, several stress tests which are beyond standard conditions as described in, for example JEDEC or AEC guidelines were performed. Especially, dynamic stress tests are important because they might trigger failure mechanisms which are not observed in static tests which follow the standard. To name only a few, the HTRB with negative gate-source voltage to stress the gate oxide or the high dv/dt tests to stress the edge termination have failed to show any significant impact on the device performance after stress. The test results show the high robustness of the CoolSiC™ MOSFET technology against temperature, voltage, moisture and dynamic stress. In the following Table 2, the tests which were executed for the CoolSiC™ MOSFET in TO247 are summarized.

Table 2 Reliability tests performed with 1200 V rated CoolSiC™ MOSFET in TO247. In none of the tests could any systematic end of life mechanism be found.

Stress test	Test conditions	Duration
HTRB	V_{DS} = 1200 V, T_{vj} = 175°C, V_{GS} = 0 V	2000 h
HTRB with negative voltage	V_{DS} = 1200 V, T_{vj} = 175°C, V_{GS} = -10 V	2000 h
HTRB with negative voltage	V_{DS} = 1100 V, T_{vj} = 175°C, V_{GS} = -15 V	1000 h
HTRB with 0x and 10x short-circuit stressed parts	V_{DS} = 960 V, T_{vj} = 175°C, V_{GS} = 0 V with initial 0x and 10x short-circuit stressed parts	1500 h
HTGS	V_{GS} = +20/-20 V constant, T_{vj} = 175°C	2000 h
HTGS with 0x and 10x short-circuit stressed parts	V_{GS} = +20/-20 V constant, T_{vj} = 175°C with initial 0x and 10x short-circuit stressed parts	1000 h
HV-H3TRB	V_{DS} = 1200 V, T_a = 85°C, RH85%	2000h
Dynamic H3TRB	T_a = 85°C, rH 85%, $V_{DC\ link}$ = 960 V, V_{GS} = +15 V/0 V, I_{L_peak} = 16 A, f_{sw} = 25 kHz, dv/dt = 70 V/ns	1000 h
Dynamic Reverse Bias (DRB)	T_a = 25°C, $V_{DC\ link}$ = 960 V, V_{GS} = +15 V/-5 V, dv/dt ~ 200 V/ns, f_{sw} = 100 kHz	1000 h

8.2 AC-HTC test procedure

In the literature, additional failure mechanisms not triggered even by the (extended) standard tests have been reported for SiC devices. These are related to the special material properties of SiC and certain application conditions [41] [42].

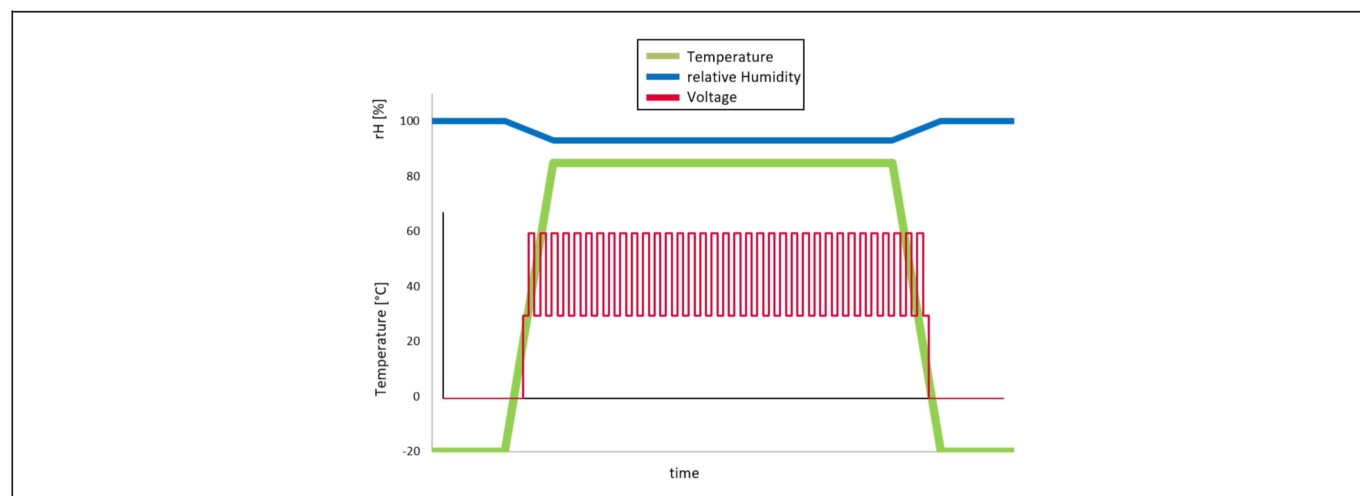

Figure 25 Schematic stress profile of an AC-HTC test cycle.

While the standard tests under T_a = 85°C/rH = 85% conditions aim to prevent condensation on the actual chip surface [39] the AC-HTC test is designed to provoke condensation and so additional, application relevant failure modes which are caused by formation of a water layer in the edge termination region. In literature, it is reported that such failure modes can be very relevant for SiC devices [41] [42]. Our SiC devices are robust against this new, material specific failure mode. This is proven by performing and passing the AC-HTC-test (alternating current – humidity and temperature cycles), a test developed in close alignment with application experts to mimic operation in the field of solar systems. A schematic stress profile is shown in Figure 25. A test cycle of several hours is divided into two different phases:

a) T_a < 0°C: Low temperature with high humidity, leading to condensation on the chips surface and a high degree of humidity in the module. To prevent self-heating and thereby dry out, no voltage is applied during this phase.
b) T_a > 0°C: When the temperature is increased up to 85°C, the device under stress is switched with higher frequencies and voltages similar to those seen in the real application.

If the passivation in the edge termination area is not sufficient, the edge termination is degraded resulting in early failures both during the test and in the application. All SiC devices in modules are therefore equipped with a new passivation stack protecting the surface under such harsh conditions and enabling AC-HTC tests lasting 120 days without any degradation visible.

To summarize, the results of long term HV-H3TRB, AC-HTC and many years of field experience of our SiC diodes with the same passivation, edge termination concepts and FIT rates comparable to Si technologies provide proof that also our CoolSiC™ MOSFET is a reliable device even under harsh field conditions in humid environments.

8.3 Power cycling seconds

To calculate expected lifetimes of semiconductor devices in the real application, the aging of the interconnection technologies has to be taken into account. This is assessed via power cycling second tests where the device is actively heated to induce a high ΔT to alter the solder and/or bond connections until a predefined change of $R_{DS(on)}$ or $R_{th(j-c)}$, the so called End of Life (EoL) criteria, is reached. Based on well known models [43], these results can be correlated to application conditions as described in the Infineon application note, derived from tests with Si devices [44].

In principal, this process is the same for SiC modules. However because SiC has a higher Young modulus than Si, the SiC chips in power modules induce a higher amount of plastic strain into the solder joint [45] during a temperature cycle. Therefore, the aging mechanism for soldered SiC chips in modules is not so much the degradation of the bond connection but dominated by the degradation of the solder layer resulting in an R_{th} increase. This is the reason why the power-cycling seconds capability of SiC is reduced compared to Si with the same interconnection technology [45]. The power-cycling curves, available on request from your local Infineon application engineering team, takes this changed aging mechanism into account, enabling the calculation of expected lifetime depending on the maximum junction temperature T_{vj} and the temperature swing ΔT following the explanations in the power cycling AN [44]. For the calculation of complete application profiles, the dependency of the aging on the load pulse duration t_{on} has to also be taken into account. This dependency is given in our recently published paper [46], showing that for our SiC devices, the same calculation models as for Si can be applied. The dependency of the cycles until end of life dependency on load pulse duration is also given in Figure 26.

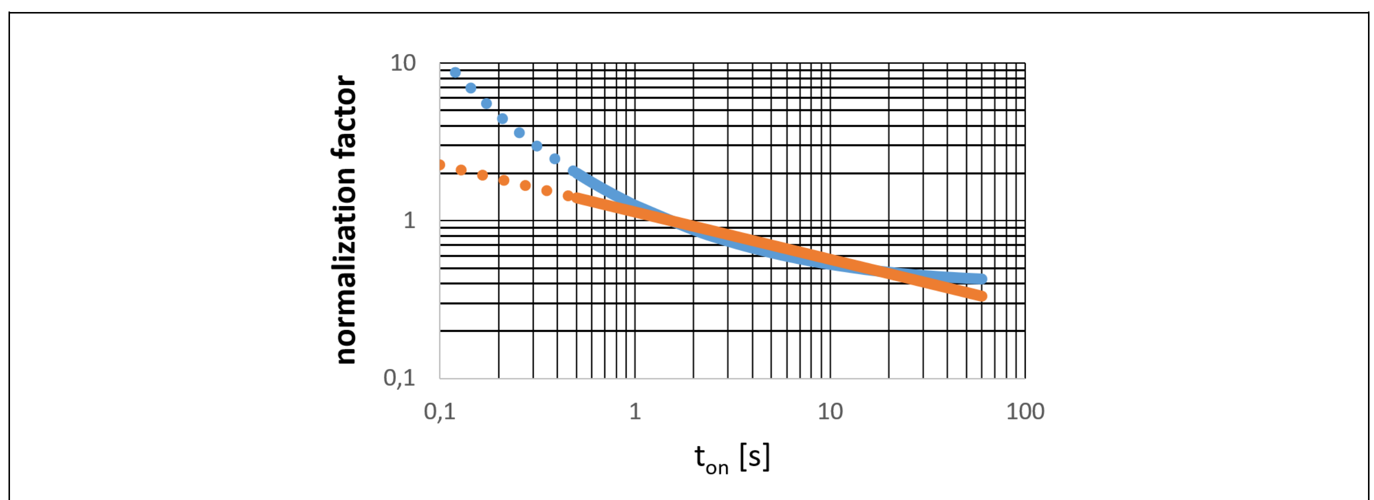

Figure 26 Correction factor N cycles overtime for a reference turn-on time of t_{on} = 1.5 s for CIPS model [44] (orange) and the adapted equation including saturation (blue). Dotted values are extrapolated, and should only be used as a guide for the eye. [46]

For all SiC technologies, the same interconnection technology and production lines are used as for Infineon Si IGBT’s and Diodes giving us decades of experience in controlling these processes and the module assembly. Another advantage of our CoolSiC™ MOSFET technology is that we do not need to use an additional, anti-parallel diode but are able to use the body diode of the CoolSiC™ MOSFET in

synchronous rectification mode. This results in applications where the device is taking current in both directions, that power is being generated in the chip during both positive and negative conduction phases of a load cycle, leading to a reduced temperature swing for each chip compared to operation of a Si IGBT and diode.

For applications requiring even higher numbers of cycles until end of life in power cycling, Infineon also has improved interconnection technologies like diffusion soldering for discrete devices [47], which can be used in future to enable the usage of our CoolSiC™ MOSFETs in other applications.

Power cycling investigations for discrete components is still a young field of research. Thus, deeper investigations have been performed in recent years to understand the failure mechanisms which occur during power cycling stress [47] [48]. One key finding is that in contrast to power modules in discrete devices bond wire lift off is the dominant failure mode today provided the die attach is done by classical solder. For the mathematical description and the relevant parameters of the degradation an equation was derived which is similar to the one which is used for power modules [48]. Independent of the chip technology (Si IGBT or SiC MOSFETs) discrete components can be described by the same equation. Several device properties have an impact on the power cycling stability so that not one parameter set can describe all products in general. Depending on device properties a separate parametrization might be necessary. For the power cycling capability of a certain device please address a request to your local Infineon AE who can help you to evaluate the expected lifetime.

8.4 Long-term application tests

SiC MOSFETs are used in a variety of different applications like EV charging stations, solar inverters or motor drives. Most of the applications can be reduced to a few basic topologies which help to define long-term application tests. The following table shows the most dominant basic topologies.

Overview of basic topologies

DC-DC converter	DC-AC converter
› Buck converter	› 1-phase
› Boost converter	› 3-phase
› H-bridge	

The main focus is on hard switching configurations because they are usually the most demanding for power semiconductors. Infineon has developed several test benches which can stress the SiC MOSFET in each of the listed configurations. These test benches enable us to run the devices under conditions that mimic the real world application. The typical testing time for reliability tests of 1000 h was extended to 6–12 months of operation to get a better understanding of the long-term behavior. The investigations have shown that the SiC MOSFET shows no indication for hot carrier injection and no systematic EOL mechanisms under these real world operating conditions.

9 Automotive qualification: an approach beyond the standard

Silicon Carbide (SiC), with its intrinsic superior physical material properties and high breakdown field, is one of the best candidates to meet the growing consensus, within the Automotive Industry, that electrification will shape the future of mobility. Infineon uses various quality categories, since SiC devices are used in both industrial and automotive applications, applied to our products. Based on our quality handbook the differences can be described as follows:

Industry

- A wide range of applications
- Longer service life of more than 5 years up to 30 years or rugged environmental condition
- Baseline qualification approach provides conformity with standards (like JESD47) and additionally robust validation accommodates for specific mission profiles if needed

Automotive

- Widely varying use conditions and loads
- Lifetime ≥ 15 years
- Quality targets at ppb level/OEM expecting no single fail
- Robustness qualification approach in applications defined in AEC Q-100/101 requirements

Automotive application profiles are now reflecting the fast pace of change in the car market and wide bandgap semiconductors are becoming popular because of the evident potential to fulfill some of the more stringent requirements. The price to pay for entry into this market is high quality coverage, translated into longer lifetime, understanding of the different failure mechanisms and new activation energies. In general the need to improve performance is becoming the norm and a way for suppliers to gain an advantage over their competition.

The evolution seen in the automotive market, especially with electrified vehicles, influences the assessment of the product quality as follows:

1. Longer stress time required from mission profiles. AEC-Q101 is then a minimum which has to be meet in all cases.
2. Design new stress conditions to cover real world application conditions and the behavior of new technologies under these conditions.
3. Robustness validation now begins at a much higher level than the standard based qualification tests.

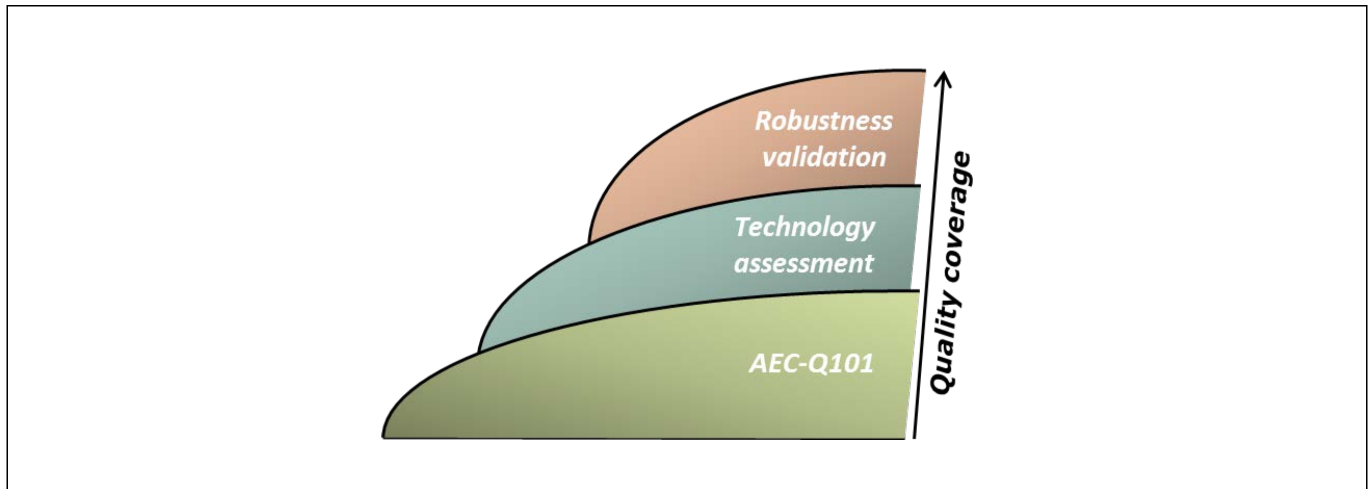

Figure 27 Best known method of how to increase the quality coverage starting from the existing automotive standards for discrete products AEC-Q101

Fulfilling the automotive norm is not sufficient anymore, the AEC-Q101 is taken as a necessary guideline but mission profiles are now requiring higher robustness, at fast switching speeds in harsh environmental conditions. All this under field strengths up to 15 times higher than the typical breakdown levels of Si-based technology.

The same high voltage product for an electrified vehicle is required to fulfill different operating modes at the same time and to be robust for each of them.

- Charging mode, up to more than 30000 hours operation at a steady high DC-link voltage
- Driving mode, with approximately 8000 operating hours, potentially at high junction temperatures and over a wide voltage range, depending on the battery performance
- Preconditioning, a feature that new xEV vehicle are exhibiting, for example heating the interior drivers space prior to using the vehicle, activated either as a timed event or remotely. This can account for 3000 operating hours

When requirement data from the AEC-Q101 is translated into equivalent stress times there is a clear mismatch between the mission profiles and the requirements of emerging applications, pointing to the need for technologies, as in the case of SiC, that go beyond the current automotive standard to fulfill harsher quality requirements.

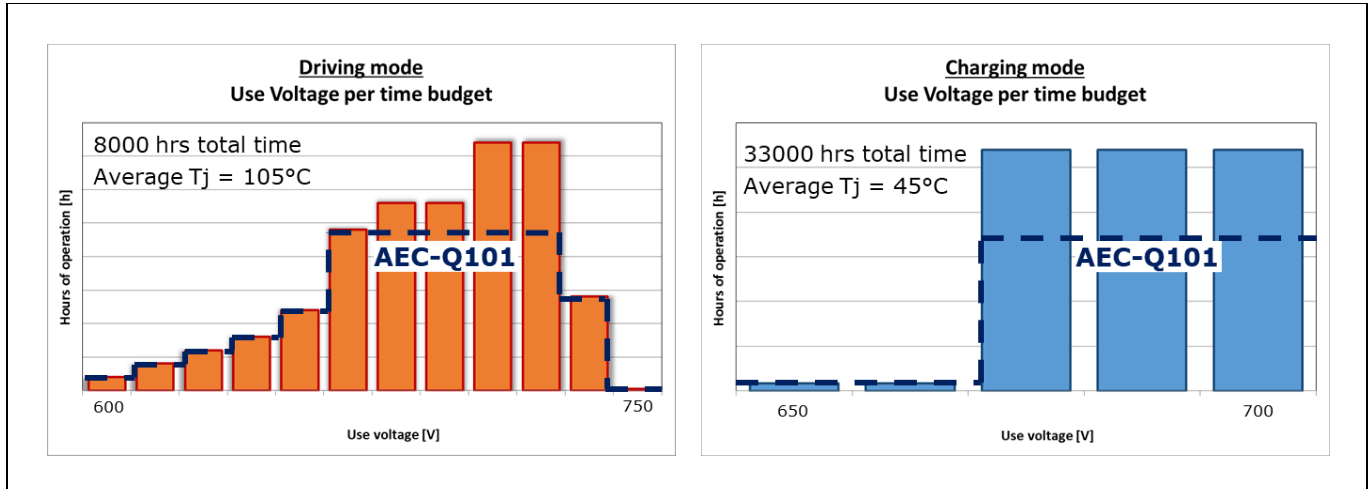

Figure 28 Mission profile for a typical xEV application (driving and charging modes). The translation of the requirements from the AEC-Q101, i.e. 1000 hours, into equivalent hours of operation shows the missing coverage of the standard

Robustness margins have consequently reduced due to the growing complexity of products and more challenging use cases: the application requirements are now set at a level where in the past robustness investigations were starting

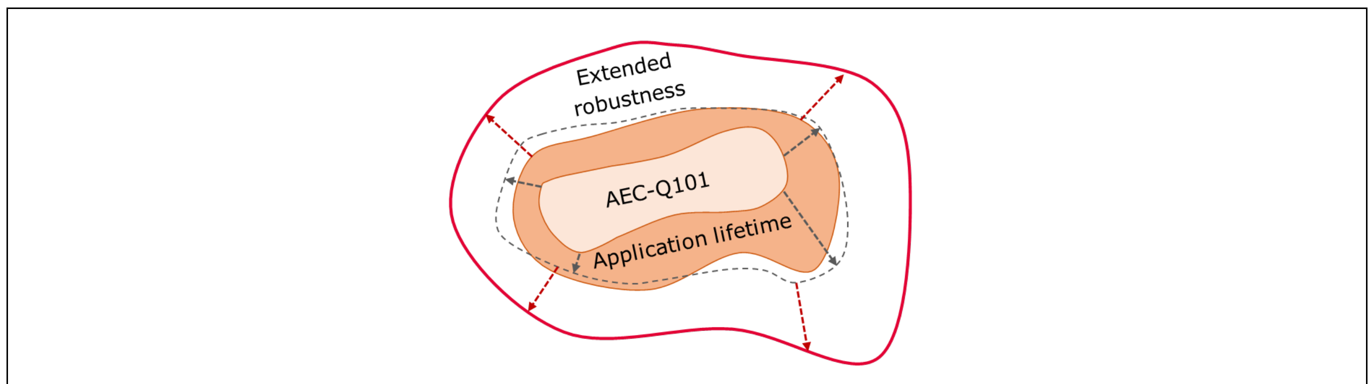

Figure 29 Extension of the robustness margins compared AEC-Q101 as a consequence of more demanding application requirements.

9.1 Higher field reliability for automotive SiC customers

Automotive markets demand extremely low dpm (defects per million) rates and no differentiation is expected between the reliability offered by a traditional Si based semiconductor and the one based on SiC technology. As such it is imperative to find a compromise between this newer technology which has not reached the maturity level of Si and an acceptable FIT number which meets the automotive application requirements.

Gate-oxide: a thicker Gate oxide allows an enhanced screening capability and consequently, the required reduction of extrinsic defects (please note chapter 3.2).

Cosmic Ray: the drift zone (epilayer) can be designed in such way to ensure higher ruggedness against cosmic radiation. Modulating the resistance of the drift layer R_{drift} enables a scaling up or down of the performance against CR.

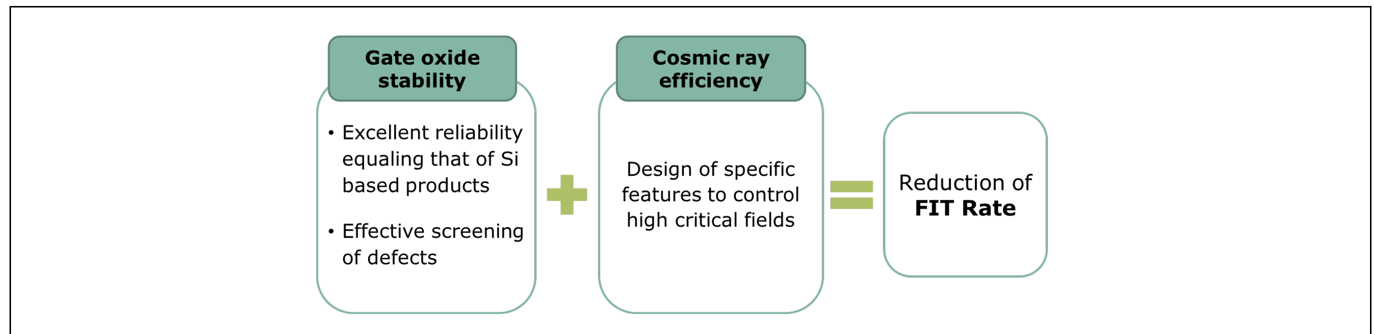

Figure 30 The FIT rate is strongly dominated by both, the gate oxide stability and the protection against cosmic radiations

9.2 No compromises on robustness against humidity for automotive parts

The constant exposure of any automotive part to variable and sometimes harsh climatic conditions makes it imperative to protect the devices against moisture penetration and consequent corrosion and/or oxidation. Similar to industrial mission profiles for outdoor applications like solar or traction for their specific environment the qualification procedures and technological measures for automotive applications need to assure extraordinary high levels of robustness.

The current version of AEC-Q101 requires a High Humidity High Temperature Reverse Bias test (H3TRB) at a maximum of 100 V, a value that obviously does not fit high voltage application where a maximum bias of up to 1200 V can occur. Given the constraints in peripheral geometry of SiC devices and the need to maximize active area, the lateral electric fields are nominally higher than with Si based parts, making SiC technologies particularly sensitive to moisture related failure mechanisms.

High Voltage H3TRB with V_{DS} = 80% V_{DSS} is a more appropriate measure to test the reliability of a SiC device against humidity. This is well justified approach considering that in many applications the operating voltages are way above the 100 V prescribed by the automotive standard (see also Table 1).

As already indicated in chapter 8.1, there is as well a dynamic behavior which can influence the reliability: the effect of charging and discharging the edge termination, typical in switching devices, is more prominent for SiC where the switching performance is markedly superior compared to Si. For this reason, e.g. a dynamic H3TRB is an possible stress test to verify that the robustness of the edge termination is not negatively affected due to continues changes of the level of the electric field induced by turning the device on and off. If the duty cycle is modulated appropriately, the dynamic H3TRB can help to address any failure mechanism related to overshoot when a fast rising time (dv/dt) occurs (higher blocking voltages, accelerated aging). Due to the similarity between several industrial and the

automotive applications regarding moisture exposure the applied qualification measures are alike as it is evident when comparing Table 1, Table 2 and Table 3.

Table 3 Selected test conditions for automotive qualification at Infineon

Qualification test conditions (examples)		
AEC-Q101	Automotive SiC (beyond AEC-Q101)	Added value
H3TRB @ 80–100 V	HV-H3TRB @ › 80% V_{DSS}	Ensure robustness against humidity under realistic application conditions
Static H3TRB @ 80–100 V	Dynamic (HV)H3TRB › f = typical switching frequency › $V_{DS,app}$	Considers the real world application usage, transient operation, dV/dt, and voltage overshoots in a high humidity climatic environment

Without applying those test procedures it would have not been possible to develop the previously mentioned innovative passivation concept to protect the edge termination against moisture penetration. Several new failure mechanisms were in fact detected and eventually mitigated thanks to HV-H3TRB and to dynamic H3TRB testing.

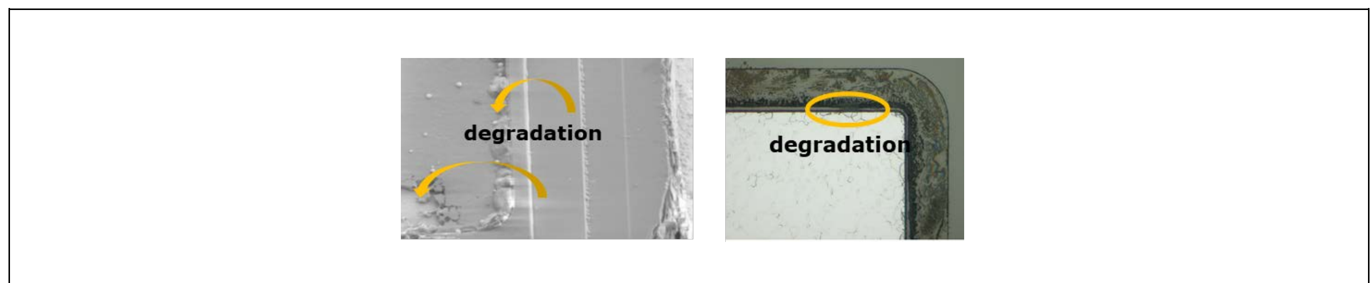

Figure 31 Failure mechanisms on a SiC edge termination test vehicle after internal physical inspection. The degradation was triggered by the HV-H3TRB, the dynamic H3TRB where the edge termination design including the passivation was not designed properly.

Only by developing the new passivation concept and repeating the enhanced humidity stresses was it possible to release the SiC technology suitable for an automotive application. Infineon was able to benefit in this process from the experience gained in the release process for many industrial products.

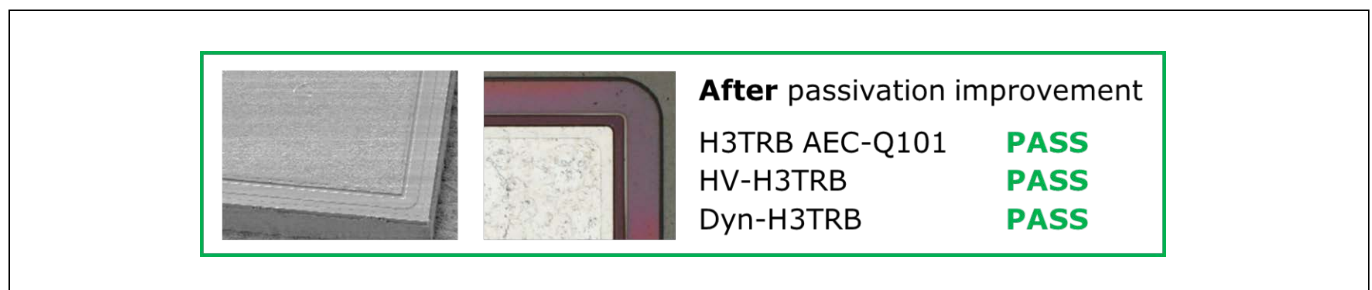

Figure 32 Edge passivation after implementing a moisture robust materials design in order to pass qualification tests under high humidity.

10 Industry standards for SiC device reliability and qualification

As detailed in this white paper, Infineon follows a comprehensive qualification regime for its CoolSiC™ devices to assure reliable performance in real world operating conditions and applications. Nevertheless, the importance for the industry to develop comprehensive standards for device qualification is unquestionable. Industry standards are set to ensure that any quality related concerns can be addressed simply and quickly without reference to the details of failure mechanisms for each supplier. Accordingly, Infineon has initiated and contributed to the establishment of a SiC focused subcommittee (JC-70.2) within JEDEC to introduce qualification guidelines and standards with regards to SiC devices. In this JEDEC effort, Infineon supports the views and approaches described in this publication. The guidelines and standards to be developed in the JEDEC committee will focus predominantly on the mentioned differences to the silicon technology and the related needs to adjust procedures accordingly. It will cover reliability testing, characterization procedures and datasheet definitions. The JEDEC work is executed in close alignment with other relevant standardization bodies like IEC or JEITA in Japan. Furthermore, via cooperation with the AEC and working groups like AQG324, for automotive power devices, Infineon ensures that coverage for both, industrial and automotive applications will be addressed.

Questions

This white paper deals with many technical topics some of which are quite complex. If there are any questions we recommend that follow up can be made through the local Infineon applications team who will be available to assist.

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