How To Survive In A World Of Evolving Serial Standards

I. Introduction

A well-worn adage tells us that "the only constant is change." Clearly this is true of serial data technology and the standards that define it. Serial architectures and protocols advance from one generation to the next, gaining performance as they go. Standards committees and working groups meet to debate evolutionary changes. And specifications—including compliance measurement specifications—evolve as new tools, technologies, and methods emerge.

How can you stay ahead of compliance requirements that will inevitably change? How can you be sure your product will comply with performance standards that are still being defined? It is a process of making assumptions, building on experience, taking some risks, and "leading the target."

Compliance is not without its costs. Interpreting the standards, purchasing measurement equipment, making the necessary measurements, and documenting the whole process... it all costs money, time, and resources. This white paper will examine some of the issues that confront serial device designers as they develop competitive, compliant devices.

II. Evolution and Uncertainty

Standards take shape after lengthy research, validation, and input from committee participants, and negotiations. Even so, change at some level is inevitable. For example, the disk drive industry saw a rapid architectural change when serial buses replaced their parallel counterparts. In contrast, the change from a "Gen I" implementation to the second generation might involve only a data rate increase and according updates to the specification. What prompts these changes?

- Industry needs or business priorities may change. For example, Infiniband arrived on the scene promising to be a near-universal connectivity and transport solution. However, simpler and more optimized niche solutions arose to challenge that presumption. Infiniband gained acceptance in server-related environments but never became the allencompassing solution it was intended to be.
- Technologies can take an unforeseen turn. One promising (and proprietary) high-speed memory architecture fell by the wayside after a rather short lifespan on the market, when Double Data Rate (DDR) devices appeared with a simpler, more open solution to the speed issue.
- Conversely, the market sometimes embraces a new technology more quickly than anticipated. An example of this is the rapid transition toward multi-lane serial configurations in PCI Express. This has implications about product characteristics as well as test requirements.
- New test methods and tools may emerge, opening the door to faster or better compliance testing. This can affect both the process (the testing procedure itself) and the achievable results, potentially causing a restatement of the electrical requirements.



But these trends are only the headlines of a larger story. Realistically, most designers face a day-to-day challenge on a very different level. The typical engineer is much more concerned with making a good showing at interoperability events—"plugfests"—and getting a proven product to market.

III. Stepping Up To the Plugfest

A plugfest is typically sponsored by an industry working group in behalf of a particular standard such as Serial ATA or PCI Express. The event brings together a community of people with an interest in the standard: product developers working with the new technology; working group members; industrywatchers and media editors; vendors of the tools and instrumentation used to measure compliance and performance.

Looking at Figure 1, we see a simplified product development cycle, from concept to announcement. The plugfest is the turning point in this continuum. It can make the difference between achieving timeto- market goals and literally "going back to the drawing board."



As the plugfest name implies, various devices are connected together to confirm their interoperability. But plugging a transmitting device into a receiving component, for example, and confirming that the arrangement "works" is not enough. Measurements must verify compliance with voltage, timing, and impedance requirements. Bit error rates must be assessed; failures pinpointed and importantly, disparities resolved. The ideal of the plugfest is to put every candidate product on the same footing with regard to test conditions, methods, and equipment.

Clearly, it is every designer's wish to pass the plugfest compliance and interoperability tests with "flying colors." The key to success here is to give the pre-compliance step its full measure of attention and diligence. At this stage, the new design has been debugged and cleaned up. Now that the device works in the basic functional sense, it is time to measure its performance against the best available knowledge about the standard.

Information, Involvement, and Preparation are the Keys To Being "Plugfest-Ready"

What is the key to staying in step with emerging standards? Actually there are several avenues open to developers.

The first and perhaps most important is "working group involvement." Many companies participate in their industries' working groups specifically to monitor and influence emerging standards. Because most standards committees base their decisions on the outcome of roll-call votes, it is not possible to anticipate the exact form the final standard will take. But the insight that comes with committee participation provides good visibility of trends and directions.

Secondly, it is often possible to capitalize on standards that already exist. Many standards have their origins in established serial protocols. For example, DisplayPort architecture draws from Serial ATA technology, though with some differences in the area of clock performance. Both the DisplayPort standards effort and the work of DisplayPort product designers can re-use much of the test expertise as well as procedures and solutions from the SATA realm.

Yet another opportunity is the plugfest "dry run" (rehearsal). At these less formal events, new implementations and ideas can be tested in a non-critical setting. Dry-runs offer a less-pressured venue to meet with colleagues facing similar compliance challenges. In addition, attendees can see, learn about, and even try out the measurement tools and procedures that will be used at the plugfest itself.

Committee Participation Helps Prepare Measurement Tools for the Plugfest Too

Measurement industry leaders, too, participate in standards groups with the intent of smoothing their customers' path toward plugfest success. Test equipment vendors, with their understanding of measurement solutions and their cross-discipline work with multiple serial standards, act as a working group's advocates for best practices in compliance testing. Tektronix participates in many standards committees with an eye toward developing timely measurement solutions and ensuring that proven methods are used wherever applicable. Tektronix solutions span many technologies and standards and leverage the common elements among all of them.

Measurement vendors who invest time and resources in committee work can use their experience to guide solutions that dovetail with evolving standards. In the case of instruments such as an oscilloscopes or BERTs this implies keeping pace with advancing performance demands, of course. But more importantly it means delivering software acquisition and analysis tools that anticipate the changing measurement needs that come with changes in the standard.

Increasingly, serial analysis relies on measurement automation, DSP, and complex math to overcome challenges such as "de-embedding" fixture effects and to maximize the observability of inaccessible signals. A case in point is Tektronix' range of jitter, eye diagram, and S-parameter measurement tools. Once an appropriate hardware platform is in place, software tools like these can adapt quickly to new developments in the standard. Some of the solutions accept plug-ins that optimize the user controls and procedures for specific standards such as PCI Express.

IV. Life Goes On After the Plugfest Ends

Over the course of an emerging standard's development, measurement tools are put to the test with every bit as much rigor as the various candidates for certification. The plugfest is the moment of truth for the measurement solutions as well as the silicon components, connectors, and cables striving for compliance. Inevitably there are competing claims, with a variety of tools and methods vying to become the "solution of choice."

It is common practice for plugfest attendees to select measurement solutions as a direct result of what they experience at the plugfest. This is a choice that can determine your course as you navigate through the continuing evolution of your industry's standards. It is a choice that can impact not only your productivity, but your product.

But it has never been easier to choose the wrong solution!

Your best insurance against making the wrong choice in measurement tools is to stand by a trusted vendor with a proven track record of participation in the working groups. At the plugfest, make an astute technical comparison of the solutions, preferably hands-on, with a healthy skepticism about unproven shortcuts and paper performance claims. Compare your device's results obtained from several measurement configurations if possible.

And in the longer term before and after the plugfest, monitor your vendors for their continuing initiative and innovation as they serve your industry.

V. Measurement Innovations and Compliance Testing

After the plugfest, refinements on any and all affected technologies continue. In particular, measurement vendors must continue to innovate if they hope to compete in the market once the standard starts to establish itself.

Tektronix innovations are confronting some of today's most difficult serial measurement challenges. These range from producing eye diagrams quickly and effectively to capturing impedance characteristics to inform SPICE models. Consider these examples:

Software Helps Eye Diagram Analysis Change With The Times

Software tools running integrally on proven measurement platforms can add efficiency to the serial measurement process and adapt as standards change. Consequently, software is a key battleground in the competition to solve compliance measurement problems of all kinds.

One such application, Tektronix' TDSRT-Eye analysis package, uses plug-ins to optimize the broader toolset to the needs of a particular standard. This approach enables users to stay in step with changes in the standards. For example, emerging PCI Express Gen II measurement specifications require the removal of de-emphasis effects from the data stream before making jitter measurements. This requirement is not presently incorporated in all standards, although it may get ported to other serial bus standards eventually. This situation is tailor-made for a plug-in solution: the PCI Express Gen II plug-in can be adapted to meet the new specification without affecting the measurement application as a whole.

Transmission Models Aid Development of Compliant Serial Devices

In a perfect world, aberration-free differential serial data signals would travel through noiseless transmission channels and arrive intact at the receiver. In the real world, things are very different. Signals can get badly degraded by high frequency losses, crosstalk, and other effects.

Increasingly, serial measurement procedures are taking this into account. One innovative approach for serial data network analysis (SDNA) applications uses TDR-based S-parameter measurement tools which are emerging as an efficient, cost-effective solution. The tools offer the performance to support uncompromised SDNA measurements with ample dynamic range for serial applications. Moreover, these platforms have gained a host of software tools to speed and simplify SDNA work.

SDNA requires time and frequency-domain characterization of the interconnect link using TDR measurements and uses the data to support SPICE modeling, eye diagram analysis, and a wide range of impedance parameters. Tools such as IConnect[™] from Tektronix can run on a sampling oscilloscope, alongside eye diagram and jitter analysis applications providing a comprehensive tool set for multi-gigabit differential serial data link characterization and compliance verification.

Solving A Jitter Measurement Problem for FB-DIMM

Not every innovation involves an entirely new product. Tektronix engineers, including some involved in several industry working groups, recently patented a new method for FB-DIMM jitter analysis. Serial FB-DIMM signals are notorious for their tendency to accumulate noise and crosstalk, with jitter as the consequence. Until now it has been very difficult to isolate the data jitter components in the midst of these degraded signals.

The new technique best described as "common mode jitter de-embedding" offers an effective solution for FB-DIMM jitter testing. The approach is based on a tool that can be found in every design department—the real-time oscilloscope.

FB-DIMM architecture maintains a reference clock channel that is separate from the data channel. Both of these paths are influenced by the same board losses; both exhibit essentially the same amount of noise and crosstalk. But the data channel also has some jitter contributed by the transmitter. This is obscured by the noise and signal degradation but nevertheless has the effect of increasing the channel's bit error rate.

The common mode jitter de-embedding technique acquires both channels and finds the differences. Since both channels carry the same noise and crosstalk, the difference between the clock channel and the data channel is the jitter value. Common mode jitter de-embedding has been proposed to the appropriate working groups and is being evaluated.

Virtual Test Points Reveal Hidden Signals

Observability is a challenge when measuring serial receiver performance. The receiver input in a serial device is an almost meaningless access point for viewing signals. This is because the serial receiver itself processes the input signal through a built-in Decision Feedback Equalization (DFE) filter designed to offset the degradation that occurs during transmission through cables, PCB traces, and connectors. The signal that goes into the active portion of the receiver—where eye diagrams and other characteristics must be evaluated—is encapsulated inside the device, inaccessible.

Tektronix DPO70000 and DSA70000 Series oscilloscopes include built-in Finite Impulse Response (FIR) filters to mimic the effect of the receiver's DFE filter. The user can load the same coefficients into the oscilloscope as were used to design the filter in the device under test. With the filter applied, the oscilloscope user can probe the input pin yet view the signal as it would be seen if the device could be probed internally. This virtual test point reveals the receiver's post-filter signal, even though the physical test point is a pin on the device package.

AWG Direct Synthesis Simplifies Receiver Jitter Measurements

Figure 2 illustrates a traditional jitter tolerance measurement setup using a pattern generator with external modulators for receiver testing. The DUT must be driven first with a setup sequence (BISTFIS), followed without interruption by a jitter-laden data signal. Clearly this is a complex arrangement, and there are some compromises in signal quality as well.



Figure 2. Modulated digital waveforms are the basis of this complex jitter tolerance measurement setup.

An arbitrary waveform generator (AWG) such as the Tektronix AWG7000 Series offers sufficient bandwidth to minimize complexity using direct synthesis techniques. Jitter in any form can be merged into the test signal itself. The effects of both random and deterministic jitter can be modeled. Moreover the AWG can incorporate the BIST-FIS instructions as part of the data, eliminating the power combiner and its effects on signal fidelity.

Observing Serial Bus Behavior in a System-Wide Context

Almost without exception, today's digital system environments include a mix of serial and parallel communication buses. Even a small, basic serial system is likely to have a debug port that delivers data in a parallel format, or parallel data buses handling internal transactions. Consequently, there is a need for tools that can capture and correlate multiple bus data streams, serial and parallel, all at once.

The logic analyzer (LA) has long been a cornerstone of parallel bus acquisition, while the protocol analyzer has performed the same role with serial data. The ideal solution would merge these capabilities and reduce complexity while offering inherent synchronization of serial and parallel data. The logic analyzer platform is a candidate but until now, serial acquisition with an LA has been possible only with the help of complex external bus support packages.

Arbitrary Waveform Generator



Figure 3. AWG-based setup for receiver jitter tolerance measurements.

Recently—and uniquely in its class—the Tektronix TLA7000 Series has gained integrated serial acquisition features for PCI Express[™] Gen I and II. Thus the TLA7000 Series becomes the sole solution that can, with one instrument, reveal serial and parallel bus interactions throughout a system. Figure 4 symbolizes the basic connection scheme for a TLA7000 Series bench top instrument equipped with a TLA7S16 Serial Analyzer module and a TLA7Dx/Ex parallel acquisition module. The probes used with the serial modules, unlike those of a protocol analyzer, are repeater-less: the data from the System Under Test does not go through a repeater that regenerates the signal, which potentially could mask some types of errors. Using repeater-less probing, the logic analyzer can view the physical layer directly.



Figure 4. Integrated logic analyzer-based tools for simultaneous serial and parallel acquisition are now available to simplify system-wide debug and validation tasks.

-	ampile	Pcse_unidir Link_Details	PCIE_Ur	PCSE_UM	PC28_U	PCSE_Ur Lane3	PCSE_Ur	PC28_UR Lanes	PCSE_Ur Lane8	PCSE_UN Lane7	PCSE_Un Lane8	PC28_Un Lanes	PCSE_Un LaneIO	PC28_Un Lane23	PCSE_UM	PC28_Un Lane13	PCSE_ur Lane14	PC28_Un Lane15	PCSE_Unidir Link_Status	PC28_ Data,
	8914 8015 8916 8917 8918 8920 8920 8921 8925 8925 8925 8925 8925 8925 8925 8925		00 00 00 00 00 00 00 00 00 00 00 00 00		00 00 00 00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00 00 00 00		00 00 00 00 00 00 00 00 00 00 00 00 00								00000000000000000000000000000000000000	00 00 00 00 00 00 00 00 00 00 00 00 00	Logne 101 e Logne	
	8937 8938 8939 8940 8941	Logical 2018 Logical 2019 Concession Dridered Set	00 00 53/2 13/2	00 00 00 00 00 00 00 00 00	00 00 00 00 00 00	00 00 00 572 502	00 00 00 00 00 00	00 00 5.72 5.52	00 00 00 07 07	00 00 507 507	00 00 00 00 00 00 00 00 00 00 00 00 00	00 00 5302 5302	80 80 90 90 90	00 00 510 510 510	80 60 97 97	00 00 510 510 510	200 200 200	00 00 510 510	Logrations	2.56
	8942 6943	DLLP: UpdateFC-NP ************************************	SOP	90	08	08	507	22	597 77	SKOP END	PAD	PAD	PAD	PAD	PAD	PAD	PAD	PAD	902	2.5G 2.5G
		HdrFC: 20h DataFC: 85Dh																		2.50
	8944	calculated OKC : 227% (6000)	500	80	20	48	01	A7	AA	END	PAD	PAD	PAD	PAD	PAD	PAD	PAD	PAD		2.50
		HdrFC: CON DATAPC: BODh																	-	2.50
	4946		00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	19915-101e	2.50
	6947 6946	Logical Idle Logical Idle	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	Logic Idle	2.50
	6949 6950	***** Electrical Idle Ordered Set ******		CON	100	CON	100	CON	11.	CON	100	CON	100	CO4	11	100	C04	1.		2.50
	6952		200	Di.	304 F9	Di.	10. WWW.Dr	21	10. WWW.Dr	018.4-	029.7-	21	028,4+	201	0.22.4+	010.7+	IL IN IS	201	8 205	2.50
	6954		012.6-	United by	unine-	United by	unine-	intra-	inine-	81 20	030.7-	8A 04.0+	Werer	aug-	06.6-	inine-	unine-	inine-		2.50
	8957	E	05.8+	aniner Ininer	unines-	and an	11416-	anine-	08. 5-	60	24/2-	and a	WATER .	018.0-	2000	and an	WATE-	andre.		2.50
	6959 6960		D0. 5-	unite-	anknes	unite-	arene-	intre-	antre-	04.0-	anteres-	uniter an	antere-	intre-	antere-	unine- unine-	arkne-	ankne-	-	2.50
	6962 6963	8	74	intra-	00.3-	intra-	Inives.	intra-	inires.	030.6+	inizes.	intra-	Inings.	025.44	ining.	intra-	017.3-	intra-		2.50
	6964 6965	**	intre-	Unine-	intre-	Unine-	inine- priner	inine-	unine-	025.6-	inine- ininer	inine-	intre- untre-	021.6-	prine-	inine-	029.7+	inine-		2.50
	6965		023.6+	WHERE -	21416-	WHITE-	and a	Ware-	44.61	01.5+	2400-	ware-	245	023, 3- EE	200	ware-	Sug-	www.cr	-	2.50
	6969	Not Aligned	018.5+	Reality	Reality	Reality	Reality	Real To	Reality	244715	Pasito	844715	Reality	Baalla	Reality	Rea 11>	anire-	Reality	Alteres	2.50
	6971	Not Aligined	CON	PTS PTC	175	875 875	175	PT5	PT5	CON	# TS	DON .	175	# 15 # 15	PT5	CON	175	CON	Aligned	2.50

Figure 5. A PCI Express trace captured by the TLA7000 Series logic analyzer.

Figure 5 depicts a page of serial data captured via the TLA7S16 module and processed for display.

Integrated serial/parallel acquisition provides a broad view of system operation and bus interactions. The logic analyzer incorporates a host of efficient analysis capabilities in a proven platform that is well-supported and familiar to most engineers. Thanks to its modularity, the instrument can be configured to acquire hundreds of parallel channels along with the serial buses. Much of what goes on inside a logic analyzer is software-based. Consequently, the analysis tools can respond readily to changing standards.

VI. Conclusion

Serial standards are bound to evolve as technologies and market demands change. While this complicates life for designers trying to introduce new products, there are ways to stay a step ahead of the changes. Participating in a working group ensures timely visibility of imminent changes. Attending plugfests and dry runs gives the designer some insight into workable solutions and methods. And choosing flexible compliance measurement platforms simplifies the transition from one serial generation to the next.

Copyright © 2007, Tektronix. All rights reserved. Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supersedes that in all previously published material. Specification and price change privileges reserved. TEKTRONIX and TEK are registered trademarks of Tektronix, Inc. All other trade names referenced are the service marks, trademarks or registered trademarks of their respective companies. 4/07 FLG/WOW 55W-20266-1

